IQS7222E DATASHEET

8 Channel Mutual / Self-capacitive and Hall-effect Touch and Proximity Controller with I²C communications interface, multi-tap combinational gestures and low power options

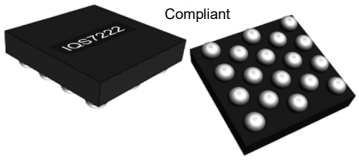
1 Device Overview

The IQS7222E ProxFusion® IC is a sensor fusion device for various multi-channel sensing elements for tap buttons, magnet Hall-effect sensing and wear detection with reference pairs. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in low power modes.

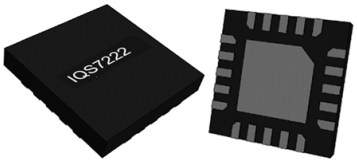
1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) / 8 (WLCSP)external sensor pad connections
- Configure up to 10 Channels using the external connections or internal sensor[i]
- External sensor options:
  - Up to 8 self capacitive buttons
  - Up to 3 self capacitive wear detection pairs (with physical reference)
  - Up to 8 mutual capacitive touch/proximity sensors
- External sensor options:
  - Hall Switch (stand / dock detect, open/close charging lid)
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Active environment tracking in activation with reference sensor
  - Debounce & Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Proximity and Touch configurable UI
  - Signal linearisation
  - Release UI
  - Hall-effect output and ultra-low power entry and wake-up
- Design simplicity
  - PC Software for debugging to obtain optimal settings and performance
  - One-time programmable settings for custom power-on IC configuration
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I2C communication interface with IRQ/RDY(up to fast plus -1MHz)
- Event and streaming modes
- Customisable user interface due to programmable memory
- Supply Voltage 1.8V(-5%)to 3.5V
- Small packages
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4mm x 0.6mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4mm pitch

RoHS2
Compliant



WLCSP18 & QFN20 package
Representation only



1.2 Applications

- SAR Compliance in Mobile devices
- Hall-effect magnet presence detection
- Waterproof switch (Hermetically sealed electronics; moveable magnet exposed to harsh environments)
- Wear Detection
- TWS UI (Tap Buttons, Press-&-hold, Grip detection)
- Low power Wake-up Buttons / Proximity
- Magnetic field change detection
- Reference tracking for compensation

1.3 Block Diagram

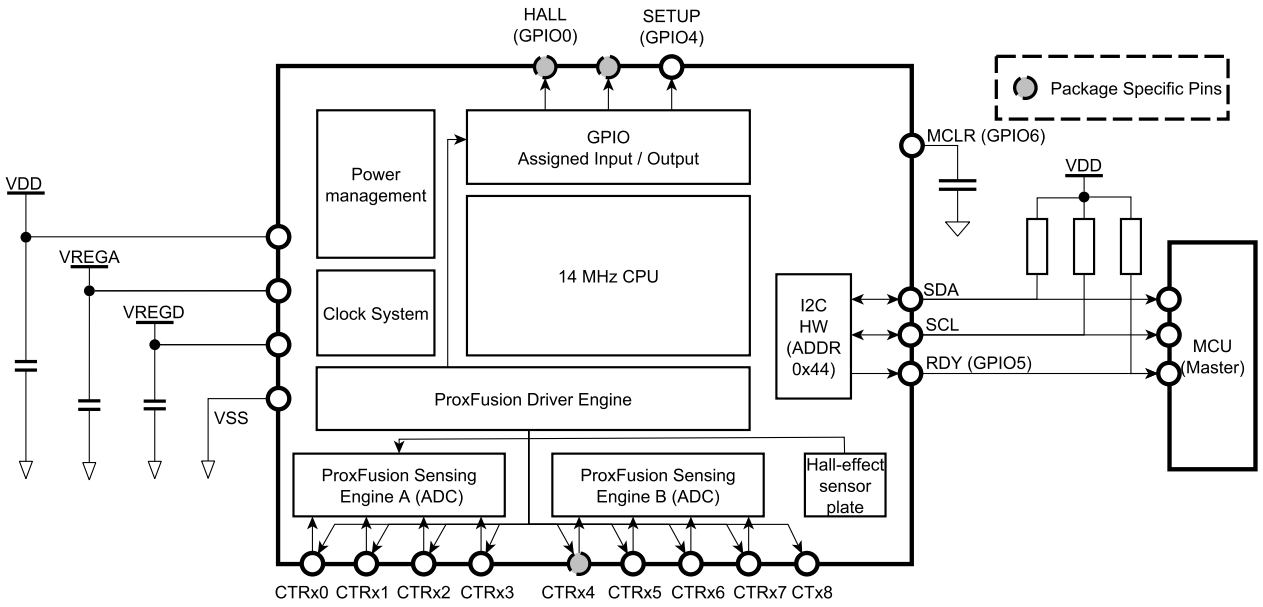


Figure 1.1: Functional Block Diagram[ii]

[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured are less than QFN20 package

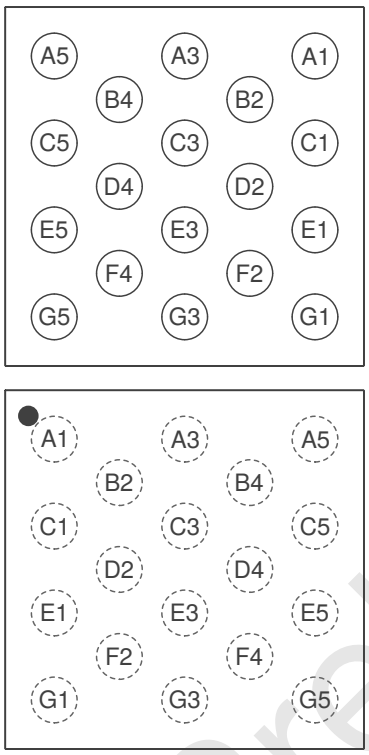
[ii] WLCSP18 packages do not have a CRx4 and combines GPIO0 and GPIO3

Contents

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

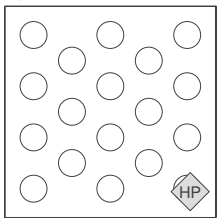
Table 2.1: 18-pin WLCSP18 Package



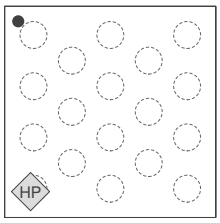
Ball-side View

Top-side View

Pin no.	Signal
A1	HALL/GPIO0/HALL/GPIO3[i]
A3	SCL
A5	MCLR
B2	SETUP/GPIO4
B4	SDA
C1	CTx8
C3	RDY
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA



Ball-side View

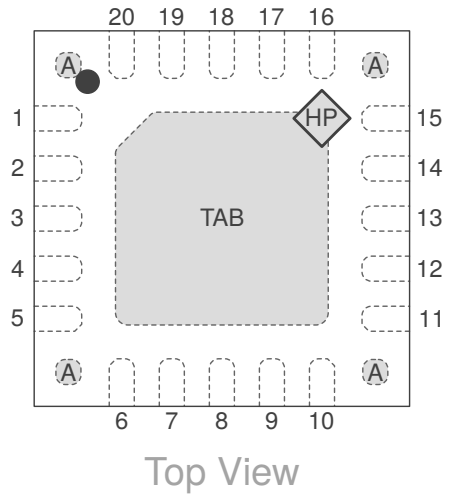


Top-side View

Area Name	Signal Name
HP	Hall Plate

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Top View

Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8
4	VREGA	14	HALL/GPIO0
5	CRx0/CTx0	15	HALL/GPIO3
6	CRx1/CTx1	16	SETUP/GPIO4
7	CRx2/CTx2	17	RDY
8	CRx3/CTx3	18	SCL
9	CRx4/CTx4	19	SDA
10	CRx5/CTx5	20	MCLR

Area name	Signal name
TAB[ii]	Thermal pad (floating)
A[iii]	Thermal pad (floating)
HP	Hall Plate

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	HALL/GPIO0	Digital		VDD
B4	19	SDA	Digital		VDD
A3	18	SCL	Digital		VDD
A1	15	HALL/GPIO3	Digital		N/A
B2	16	SETUP/GPIO4	Digital		VDD
C3	17	RDY	Digital		VDD
A5	20	MCLR	Digital		VDD

[i] Please note that HALL/GPIO0 and HALL/GPIO3 are connected together in the WLCSP18 package.
[ii] It is recommended to connect the thermal pad (TAB) to VSS.
[iii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iv]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8	C1	13	O	CTx8 pad
GPIO	HALL/GPIO0	A1	14	O	Hall status output. Push-pull, active low output pin configuration.
	HALL/GPIO3	A1	15	-	Floating undefined. Shared pin connection with HALL/GPIO0 in WLCSP18 package.
	SETUP/GPIO4	B2	16	O	Setup complete indication. Push-pull, active low output pin configuration. HIGH when device has reset and waiting for setup. LOW when device setup complete bit is set and executing conversions.
	RDY	C3	17	O	RDY pad
	MCLR	A5	20	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA	B4	19	IO	I^2C data
	SCL	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iv] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Reference Schematic

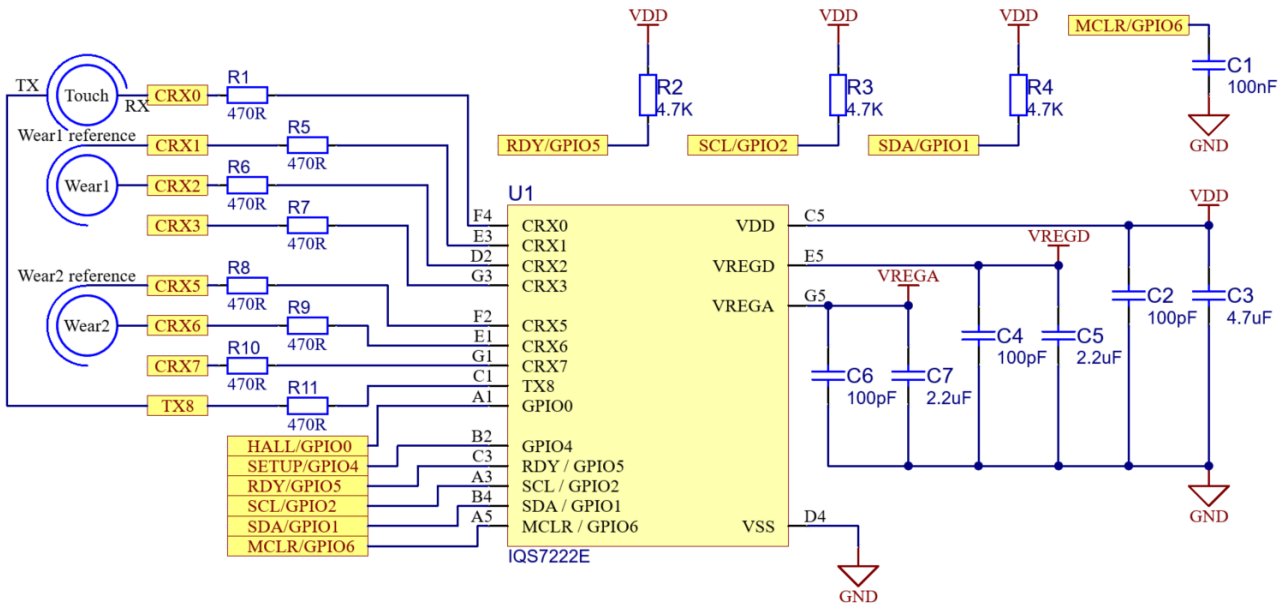


Figure 2.1: WLCSP Package Reference Schematic: Self & Mutual Capacitance Touch Button, 2 Wear & Reference pairs, 2 additional sensors & Hall-effect

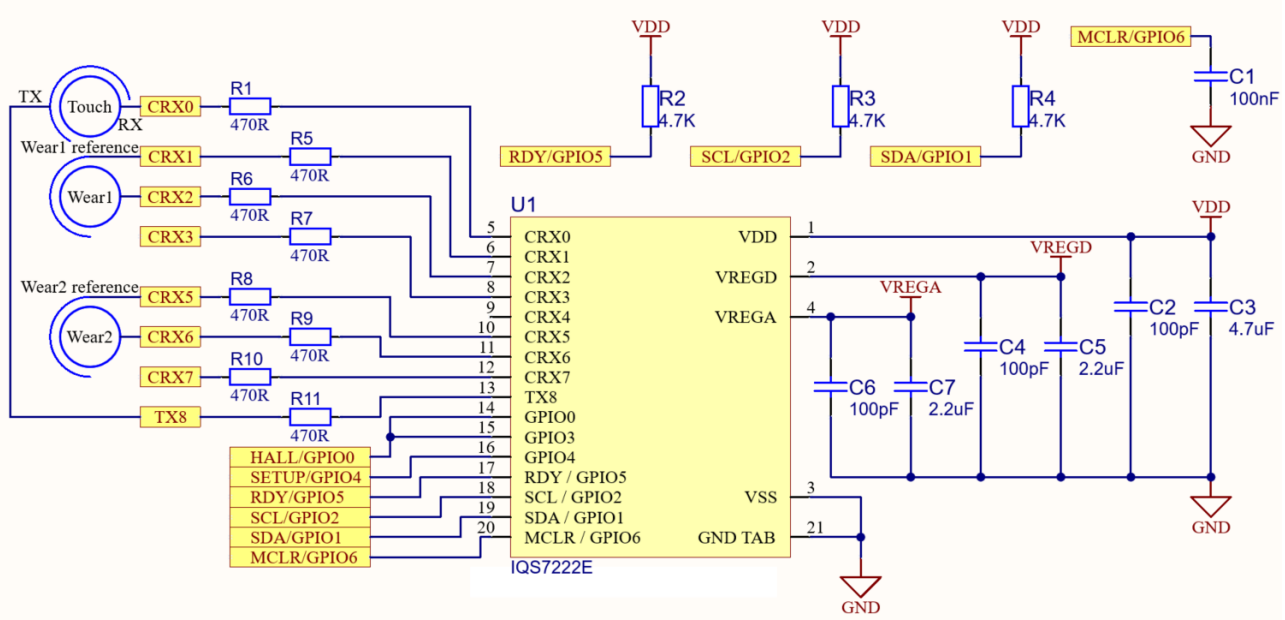


Figure 2.2: QFN20 Package Reference Schematic: Self & Mutual Capacitance Touch Button, 2 Wear & Reference pairs, 2 additional sensors & Hall-effect

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.5 V max)	V
Storage temperature, T_{stg}	–40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz	1.71		3.5	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	2×C_{VREGA}	3×C_{VREGA}		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR≤ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR≤ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx–CRx}$	Capacitance between Receiving and Transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, f_{xfer} = 1 MHz Mutual-capacitance mode, f_{xfer} = 4 MHz			 100[ii] 25[ii]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Hall Effect Sensing Characteristics

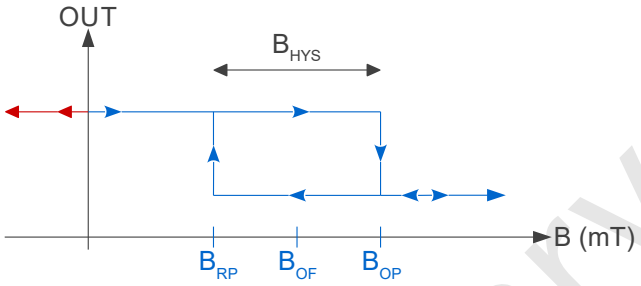


Figure 3.1: Magnet Trigger Level Description (Active Low Output)

Table 3.4: Example Power-on Magnet Detection Options

Hall Sensor Setup	Output Type	B_{RP} (mT)	B_{OP} (mT)	B_{HYS} (mT)	B_{RP} and B_{OP} Accuracy (mT)
					–10 °C to 80 °C
Threshold example 1	Direct	2.1	3	0.9	27%
Adjustable Threshold	I^2C/Direct	0 – 100% of B_{OP} (default 95%)	Software register	0 – 100% of B_{OP} (default 5%)	TBD

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.
[ii] RCx = 0 Ω.
[iii] Please note that the maximum values for Cp and Cm are subject to this ratio.
[iv] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
[v] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.
[vi] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

3.5 Current Consumption

Hall-effect UI Setup: ATI Target = 1200, F_{xfer} = 7MHz (fixed)
Self-capacitive Channel Setup: ATI Target = 512, F_{xfer} = 500kHz
Mutual capacitive Channel Setup: ATI Target = 512, F_{xfer} = 1MHz
Interface Selection: Event mode

Power mode	Active channels	Report rate (Sampling period) [ms]	Typical Current [µA]	
			1.8V	3.3V
Normal Power Mode (NP)	Hall-effect alone (full UI operational)	16	219	220
	Self-capacitive (8 channels; Hall full UI)	16	431	433
	Mutual Capacitive (8 channels; Hall full UI)	16	566	568
Low Power Mode (LP)	Hall-effect (only)	100	38	39
	Self-capacitive (8 channels; Hall full UI)	100	70	71
	Mutual Capacitive (8 channels; Hall full UI)	100	92	93
Ultra-low Power Mode (ULP)	Hall wake-up: (Hall single plate directional conversion)	200	5.4	5.6
	Proximity wake-up: (Hall single plate directional conversion; 2 channels distributed self capacitive)	200	8.8	10.4
	Hall-effect (single plate directional conversion; 8 channel capacitive update every 32th cycle)	200	36	37

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s			1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9			

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

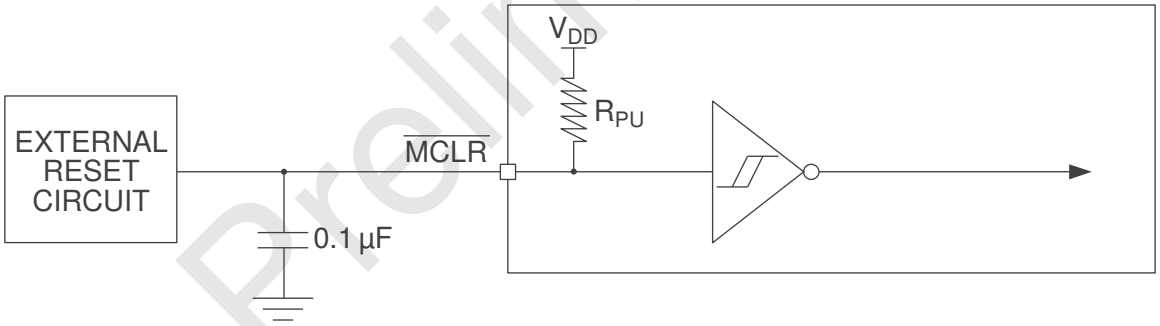


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	3500	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA			0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2			V
V_{IL}	Input low voltage				VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7			V
C_{b_max}	SDA & SCL maximum bus capacitance				550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	1.8 V, 3.3 V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	1.8 V, 3.3 V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START	1.8 V, 3.3 V	0.26			µs
$t_{HD,DAT}$	Data hold time	1.8 V, 3.3 V	0			ns
$t_{SU,DAT}$	Data setup time	1.8 V, 3.3 V	50			ns
$t_{SU,STO}$	Setup time for STOP	1.8 V, 3.3 V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter	1.8 V, 3.3 V	0		50	ns

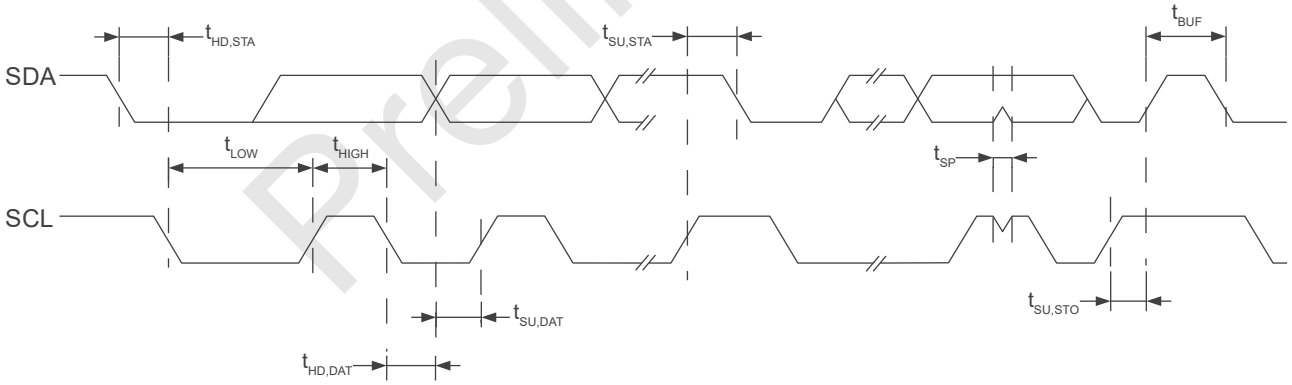


Figure 4.2: I²C Mode Timing Diagram

[i] Refers to HALL/GPIO0, HALL/GPIO3, SETUP/GPIO4, and RDY pins.

5 ProxFusion® Module

The IQS7222E contains dual ProxFusion® modules that uses patented technology to measure and process the sensor data. Two modules ensure a rapid response from multi-channel implementations. The multiple touch, proximity and Hall output are the primary output from the sensor.

5.1 Channel Options

Self-capacitance, Mutual capacitance, Reference tracking and Hall-effect designs are possible with the IQS7222E.

Table 5.1: Sensor Cycle and channel allocation

Cycle number:	0	1	2	3	4	5	6
Channel(s):	Hall		CH0	CH1	CH2 & CH5	CH3 & CH6	CH4 & CH7
Recommended sensor mode:	Hall-effect		Self/Mutual capacitive				
Channel UI:	Hall normal plate conversion	Hall inverse plate conversion	Tap Gesture		Wear/Reference		General

- Capacitive sensing design guide: AZD125
- Mutual capacitance button layout guide: AZD036
- IQS7222x User guide: IQS7222x User guide
- User interfaces application note: AZD137

5.2 Power Mode and Mode Timeout

The IQS7222E offers 3 power modes:

- Normal power mode (NP)
  - Flexible sensor sampling-/scan rate.
- Lower power mode (LP)
  - Flexible idle sampling-/scan rate.
  - Typically set to a slower rate than NP.
- Ultra-low power mode (ULP)
  - Optimised firmware setup.
  - Intended for wake-up on Hall prox threshold trigger (state exit/de-activation), enabling immediate alternative sensors/button response for an approaching/active user.
  - ULP mode can only be entered if Hall touch state is active and remains stable.
  - ULP mode only samples the Hall-effect channel (either cycle 0 or -1 will automatically be selected for sampling the lowest raw counts for optimal power efficiency).

In order to optimise power consumption and performance, power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time know as the "mode timeout". The value for the power mode to never timeout (i.e the current power mode will never progress to a lower power mode), is 0x00.

5.3 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to charge transferred into the ProxFusion engines, and all outputs are derived from this.

5.3.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit *(Maximum counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.4 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.4.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0xA0, bit3).

5.5 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and magnetic field intensity, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

5.6 Automatic Re-ATI

5.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7222E, a status bit will set momentarily to indicate that this has occurred.

5.6.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.16.

$$\textbf{Re-ATI Boundary}_{\textbf{default}} = \textbf{ATI target} \pm (\tfrac{1}{8}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and that the and the default boundary value is 1/8*800 = 100. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\textbf{Reference} > 900 \textbf{ or Reference} < 700$$

The ATI algorithm executes in a short time, so goes unnoticed by the user.

5.6.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

6 Sensing Modes

6.1 Mode Timeout

Hall effect sensing is an internal sensing option that requires no external sensor pin/circuit. The Hall-effect switch UI measures the magnetic field induced on the hall plate of the IC and is, by default, active (cycles 0 & -1). The Hall UI uses two conversions to determine the magnetic field strength and direction acting on the Hall plate. Using two conversions ensures that the ATI (refer to section 5.5) can still be used from power-on in the presence of a magnet or static magnetic field. An inverted conversion allows the capability of calculating a Hall reference value which will always be the same regardless of the presence, strength or direction of a magnetic field. Enabling the UI will enable the IC to display the effects of the magnet by reading the Hall UI data and related output registers.
The Hall effect UI is used for detection of magnetic field strength variations.

$Hall_{DeltaCounts}$ is the Hall UI output, calculated using:

$$Hall_{DeltaCounts} = \frac{Counts_{Normal} - Counts_{Inverse}}{2} * \frac{Counts_{Absolute} * Hall_{numerator}}{Hall_{denominator}}$$

$Hall_{Reference}$ serves as a reference for the Hall-effect (after power-on or an ATI execution)

$$Hall_{Reference} = \frac{2}{\frac{1}{Counts_{Normal}} + \frac{1}{Counts_{Inverse}}}$$

The settings applicable to Hall UI according to the standard UI are:

- Cycle 0 & -1:
  - ProxSensor input = Hall normal / Hall inverted plate
  - Frequency fraction = 127 (required)
  - Frequency period = 0 (7MHz)
  - Inactive sensor Rx's = Grounded (VSS)
- Hall settings
  - Hall bias current
  - Hall offset current
  - Hall boost gain
  - Hall numerator
  - Hall denominator (32-bit length composed of two 16-bit words)
  - Hall absolute current configuration (fixed setup use of 750 µA)
- Hall UI settings
  - Prox threshold (in unit of Counts)
  - Touch threshold (as a fraction of the LTA value)
  - Debounce samples required for entry
  - Debounce samples required for exit
  - Touch Hysteresis for release (as a fraction of the touch threshold)

The sensitivity of the sensor is determined by the Hall plate, the biasing current applied to the Hall plate, and the offset current applied to the op-amp output. All these parameters are configured by default settings and tuned during run-time ATI. The boost gain bit will improve the sensitivity of the Hall plate by producing a greater output current for a given magnetic field. The biasing and offset current settings both have level (coarse) and trim (fine) values for making accurate adjustments.

The recommended Hall bias current is 750 µA (register value of 0x9000). The Hall offset current is adjusted by the ATI functionality of the IQS7222E based on the operating magnetic field environment. It is not recommended for the user to modify either the hall biasing or offset current settings

The Hall Absolute current channel allows ATI to be performed using a known absolute current configuration as reference input to the Hall-effect measurement circuit. It provides the required reference to account for Hall-effect plate gain and operation amplifier offsets.

6.2 Mode Timeout

In order to optimise power consumption and performance, power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time know as the "mode timeout".

6.3 Count Filter

6.3.1 IIR Filter

The IIR filter applied to the digitised raw input offers various damping options as defined in Table A.24 to Table A.26.

Damping factor = Beta/256

7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Below, some are described, the other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*, if it becomes set again, the master will know a reset has occurred, and can react appropriately.

While *Reset* bit remains set:

- The device will not be able to enter into I^2C Event mode operation (i.e. streaming communication behaviour will be maintained until the Reset bit is cleared)
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

7.2.2 Software Reset

The IQS7222E can be reset by means of an I^2C command (*Soft Reset*).

8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific settings are exported and can be written to the device by the master after every power-on reset.

8.2 Start-up default configuration

The device is programmed with the application firmware, bundled with settings specifically configured for the current hardware as described in Section 8.1. After power-up the device will automatically use the settings and perform the configuration/setup accordingly.

8.3 Setup complete (SETUP) Output

The setup complete output (SETUP) will produce an active LOW output when the host is done with device initialisation and the setup complete bit (0xA0 bit 7) has been set to start conversions and processing. Any device reset occurrence will clear the bit (return to default) with the SETUP output HIGH (awaiting host setup and subsequent setup complete confirmation).

8.4 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.

8.5 Tap Gestures

The IQS7222E has on-chip gesture recognition features for single finger tap and press-&-hold gestures. The following gestures are supported by the device:

- Single tap
- Double tap
- Triple tap
- Press-&-hold

When a gesture event occurs, the relevant bits will be set in the gesture status register (0x14). The gesture configuration registers (0x8000 - 0x8004) must be set to detect gestures for a selected channel (either CH0 or CH1 or a combination of both) and to determine the timing configuration. For the IQS7222E gesture state machine to determine a tap gesture a touch input must be received at the selected channel that exceeds the minimum tap time while not exceeding the maximum tap time. The tap delay parameter defines the maximum duration between tap gestures to determine if a double or triple tap gesture is given as input. To detect a press-and-hold gesture a touch input must be received at the selected channel for a duration that exceeds the minimum hold time parameter.

8.6 RF Immunity

The IQS7222E has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100pF in parallel with the 2.2μF ceramic on V_{REG}. Place a 2.2μF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470Ω-1kΩ. PCB ground planes also improve noise immunity.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7222E supports the following:

- *Fast-mode-plus* standard I2C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7222E implements 8-bit addressing with 2 data bytes at each address with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The default 7-bit device address is 0x48 (’01001000’). The full address byte will thus be 0x91 (read) or 0x90 (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement 16-bit addressing scheme.

9.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to only address each Block as an 8-bit address, and then continue to clock into the next address locations. For example, address 0xE000 might be the address where certain settings are located. If you thus do the following, you will read the setting values from address 0xE000 to 0xE003:

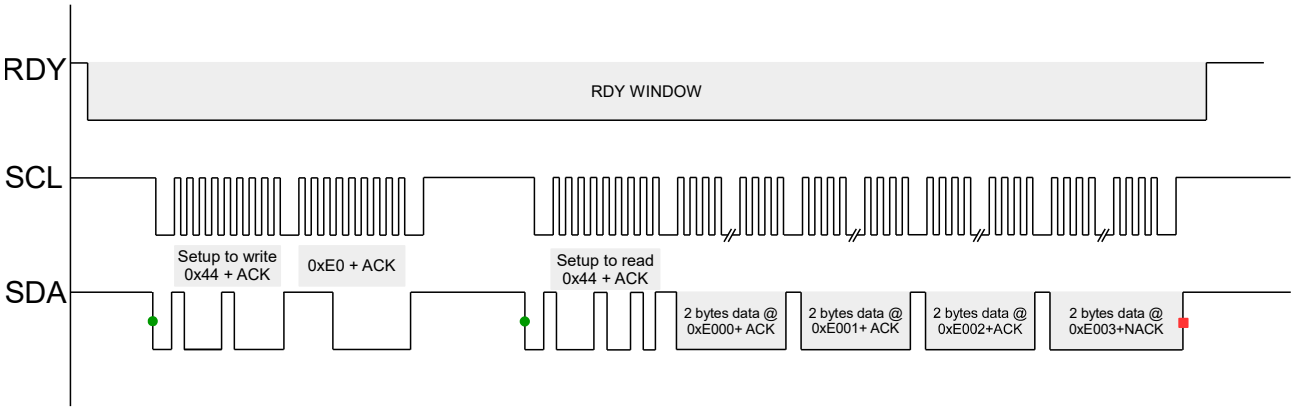


Figure 9.1: Extended 16-bit Addressing for Continuous Block

However, if you need to address a specific byte in that extended memory map space, then you will need to address using the full 16-bit address (note the 16-bit address is high byte first, unlike the data which is low byte first):

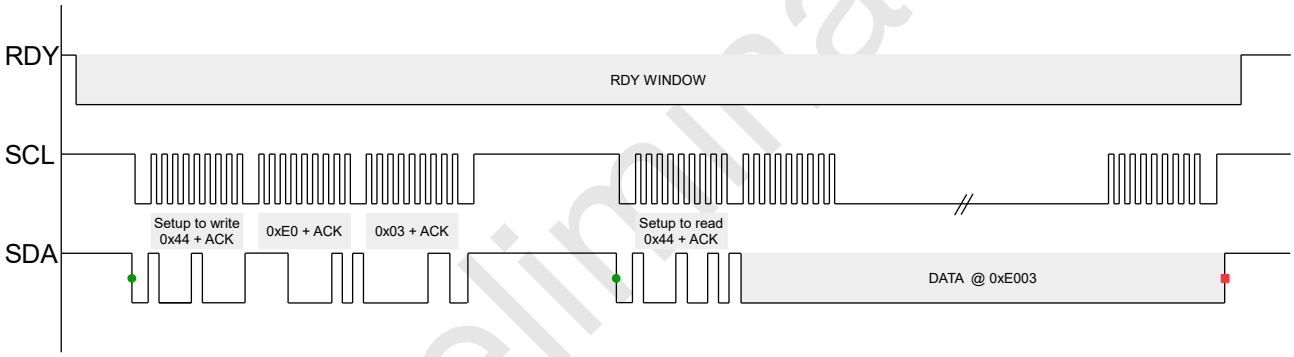


Figure 9.2: Extended 16-bit Addressing for a Specific Register

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive, however the corresponding data was missed/lost, and this should be avoided. The default I²C timeout period is set to 500ms and can be adjusted in register 0xAB.

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0xAF) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

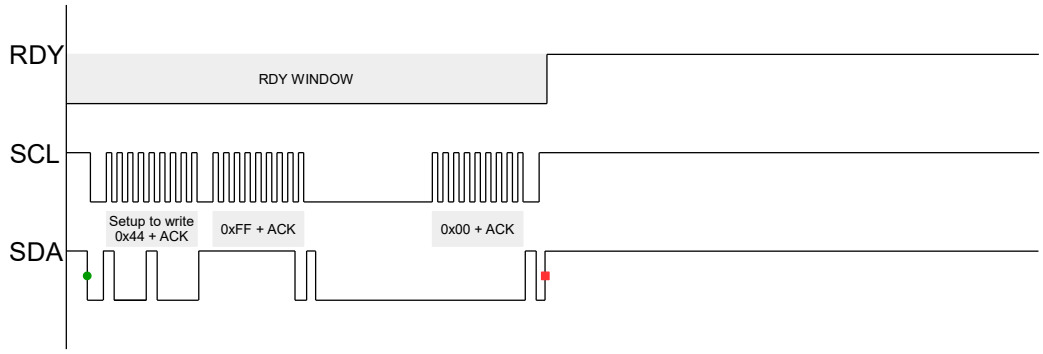


Figure 9.3: Force Stop Communication Sequence

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected.

9.9 Invalid Communication Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e., while RDY = '1'/HIGH).

9.10 I²C Communication Interface modes

9.10.1 Streaming Mode Communication

Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register 0xA4 (normal power), register 0xA6 (low power) and register 0xA8 (ultra-low power) respectively.

9.10.2 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed (Event Mode). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

The device cannot enter event mode if the following requirements are not met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the System status flag.

- Events must be serviced by reading from the *Events* register 0x11 to ensure all events flags are cleared otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode

9.10.3 Stream-In-Touch Mode Communication

Stream-in-touch is a hybrid communication mode between streaming mode and event mode. The device follows event mode I^2C protocol but when a touch is registered on any channel, the device enters streaming mode temporarily until all touch flags are cleared.

9.10.4 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.2 and Table A.3:

- Power mode change
- Prox event
- Touch event
- ATI error
- ATI active
- ATI event
- Tap gesture events
  - Single tap
  - Double tap
  - Triple tap
- Press-&-hold event

9.10.5 Force Communication

In streaming mode, the IQS7222E I^2C will provide Ready (RDY) windows at intervals specified in the power mode report rate . Ideally, communication with the IQS7222E should only be initiated in a Ready window but a communication request described in figure 9.4 below, will force a Ready window to open. In event mode Ready windows are only provided when an event is reported and a Ready window must be requested to write or read settings outside of this window. The time between the communication request and the opening of a RDY window (t_{wait}), is dependent on the report rate of the current power mode. $\leq t_{wait} \leq$ can extend up to the current report rate $+20\%$ due to variability in the clock. Example, if a report rate of 100ms is chosen, the report rate may vary between 80ms and 120ms.

There is a possibility of a communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period. However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional precautionary measure, the IC can be reset using the MCLR pin and reinitialised if there is no response after a specified number of retries.

A force communication request should be avoided while RDY is in the LOW state. If a communication request is sent at the exact moment when an event causes RDY to go low, the window will close again after sending the I^2C STOP signal. In such a scenario, the device will provide an invalid communication response (0xEE) because the host is attempting to read from the device outside of a communication

window (i.e. while RDY is high). To prevent this issue, it is recommended to read the product number during each ready window to ensure that the response received is valid.

A slight delay may occur in receiving an acknowledgement (ACK) when attempting force communication while the device is in an internal lower power mode with certain peripherals switched off. This delay can occur regardless of the state of the current system power mode.

The communication request sequence is shown in figure 9.4 below.

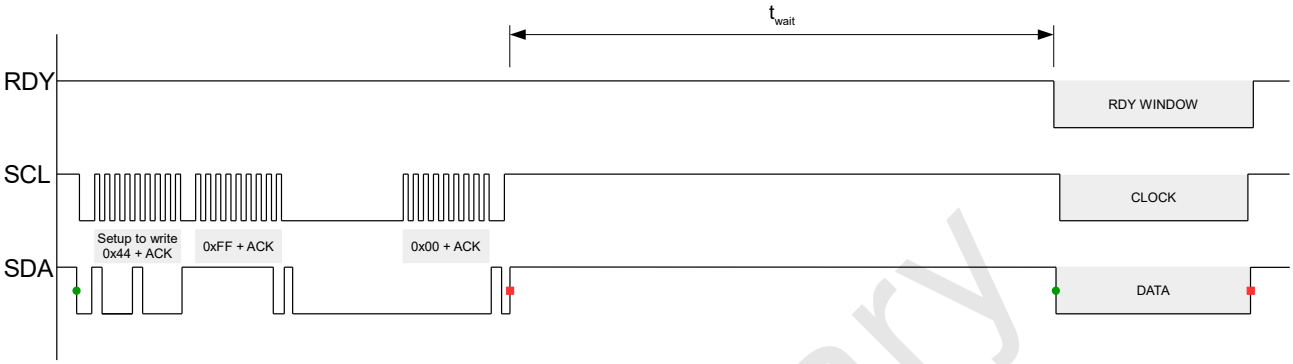


Figure 9.4: Force Communication Sequence

9.10.6 Program flow diagram

The program flow for event mode communication is shown in 9.5

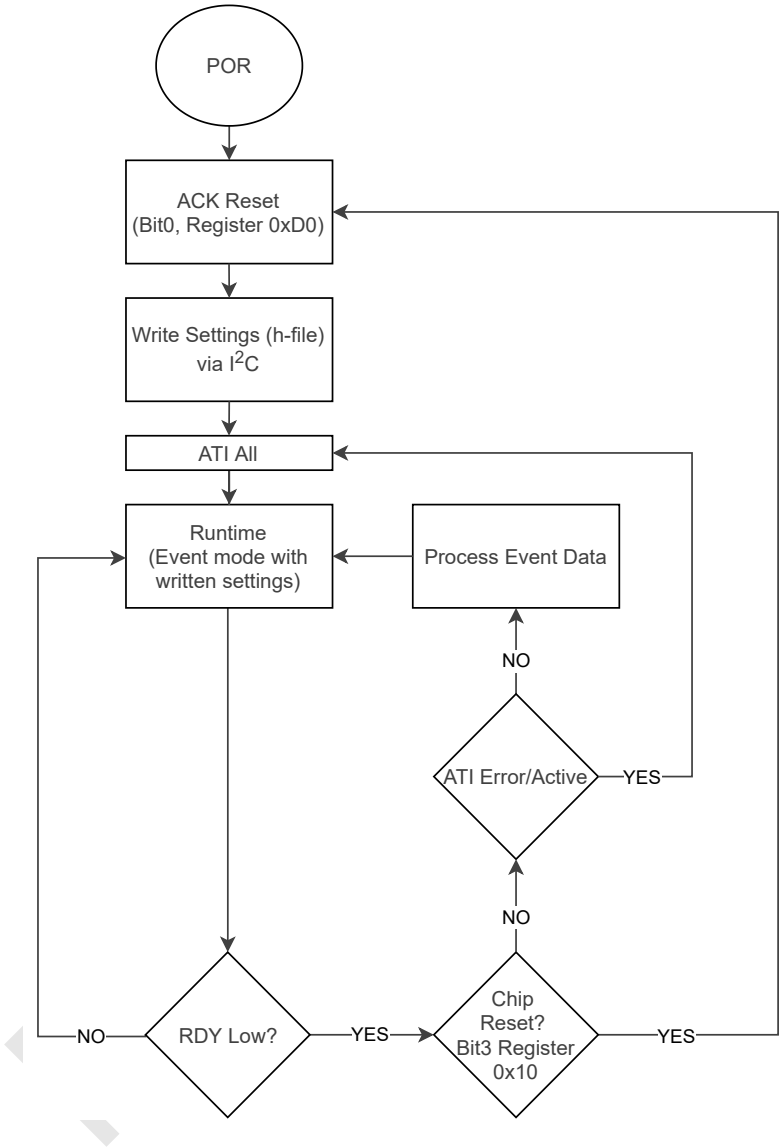


Figure 9.5: Program Flow Diagram

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only		
0x10	System Status	See Table A.2
0x11	Events	See Table A.3
0x12	Prox Event States	See Table A.4
0x13	Touch Event States	See Table A.5
0x14	Gesture Event States	See Table A.6
Read Only	**Channel Counts**	
0x20	Channel 0 Counts	16-bit value
0x21	Channel 1 Counts	
0x22	Channel 2 Counts	
0x23	Channel 3 Counts	
0x24	Channel 4 Counts	
0x25	Channel 5 Counts	
0x26	Channel 6 Counts	
0x27	Channel 7 Counts	
0x28	Hall Delta Counts	
0x29	Hall Normal Plate Counts	
0x2A	Hall Absolute Current Counts	
Read Only	**Channel LTA**	
0x30	Channel 0 LTA	16-bit value
0x31	Channel 1 LTA	
0x32	Channel 2 LTA	
0x33	Channel 3 LTA	
0x34	Channel 4 LTA	
0x35	Channel 5 LTA	
0x36	Channel 6 LTA	
0x37	Channel 7 LTA	
0x38	Hall Reference	
0x39	Hall Inverse Plate Counts	
0x3A	Hall ULP Counts	
Read-Write	**Release UI LTA & Delta Snapshots**	
0x40	Channel 0 Activation LTA	16-bit value
0x41	Channel 1 Activation LTA	
0x42	Channel 2 Activation LTA	
0x43	Channel 3 Activation LTA	
0x44	Channel 4 Activation LTA	
0x45	Channel 5 Activation LTA	
0x46	Channel 6 Activation LTA	
0x47	Channel 7 Activation LTA	
0x48	Channel 0 Delta Snapshot	
0x49	Channel 1 Delta Snapshot	
0x4A	Channel 2 Delta Snapshot	
0x4B	Channel 3 Delta Snapshot	
0x4C	Channel 4 Delta Snapshot	
0x4D	Channel 5 Delta Snapshot	
0x4E	Channel 6 Delta Snapshot	
0x4F	Channel 7 Delta Snapshot	

Read-Write	Cycle Setup	
0x5000	Cycle Setup 0	See Table A.7
0x5001		See Table A.8
0x5002		See Table A.9
0x5100	Cycle Setup 1	See Table A.7
0x5101		See Table A.8
0x5102		See Table A.9
0x5200	Cycle Setup 2	See Table A.7
0x5201		See Table A.8
0x5202		See Table A.9
0x5300	Cycle Setup 3	See Table A.7
0x5301		See Table A.8
0x5302		See Table A.9
0x5400	Cycle Setup 4	See Table A.7
0x5401		See Table A.8
0x5402		See Table A.9
0x5500	Cycle Setup 5	See Table A.7
0x5501		See Table A.8
0x5502		See Table A.9
0x5600	Cycle Setup 6	See Table A.7
0x5601		See Table A.8
0x5602		See Table A.9
0x5700	Global Cycle Setup	See Table A.10
0x5701	Coarse and Fine Multiplier Preloads	See Table A.11
0x5702	Compensation Preload	See Table A.12
Read-Write	**Button Setup - Thresholds, Hysteresis and Debounce**	
0x6000	Button Setup 0	See Table A.13
0x6001		See Table A.14
0x6002		See Table A.15
0x6100	Button Setup 1	See Table A.13
0x6101		See Table A.14
0x6102		See Table A.15
0x6200	Button Setup 2	See Table A.13
0x6201		See Table A.14
0x6202		See Table A.15
0x6300	Button Setup 3	See Table A.13
0x6301		See Table A.14
0x6302		See Table A.15
0x6400	Button Setup 4	See Table A.13
0x6401		See Table A.14
0x6402		See Table A.15
0x6500	Button Setup 5	See Table A.13
0x6501		See Table A.14
0x6502		See Table A.15
0x6600	Button Setup 6	See Table A.13
0x6601		See Table A.14
0x6602		See Table A.15
0x6700	Button Setup 7	See Table A.13
0x6701		See Table A.14
0x6702		See Table A.15
0x6800	Hall UI Setup	See Table A.13
0x6801		See Table A.14

0x6802		See Table A.15
0x6900	Reserved	See Table A.13
0x6901		See Table A.14
0x6902		See Table A.15
Read-Write	**Channel Setup- ATI Parameters, Reference Channel and Rx Select**	
	Channel 0	
0x7000	CRX Select and General Channel Setup	See Table A.16
0x7001	ATI Base and Mode	See Table A.18
0x7002	ATI Target	See Table A.19
0x7003	Fine and Coarse Multipliers	See Table A.20
0x7004	ATI Compensation	See Table A.21
0x7005	Reference Channel Settings 0	See Table A.22
0x7006	Reference Channel Settings 1	See Table A.23
	Channel 1	
0x7100	CRX Select and General Channel Setup	See Table A.16
0x7101	ATI Base and Mode	See Table A.18
0x7102	ATI Target	See Table A.19
0x7103	Fine and Coarse Multipliers	See Table A.20
0x7104	ATI Compensation	See Table A.21
0x7105	Reference Channel Settings 0	See Table A.22
0x7106	Reference Channel Settings 1	See Table A.23
	Channel 2	
0x7200	CRX Select and General Channel Setup	See Table A.16
0x7201	ATI Base and Mode	See Table A.18
0x7202	ATI Target	See Table A.19
0x7203	Fine and Coarse Multipliers	See Table A.20
0x7204	ATI Compensation	See Table A.21
0x7205	Reference Channel Settings 0	See Table A.22
0x7206	Reference Channel Settings 1	See Table A.23
	Channel 3	
0x7300	CRX Select and General Channel Setup	See Table A.16
0x7301	ATI Base and Mode	See Table A.18
0x7302	ATI Target	See Table A.19
0x7303	Fine and Coarse Multipliers	See Table A.20
0x7304	ATI Compensation	See Table A.21
0x7305	Reference Channel Settings 0	See Table A.22
0x7306	Reference Channel Settings 1	See Table A.23
	Channel 4	
0x7400	CRX Select and General Channel Setup	See Table A.16
0x7401	ATI Base and Mode	See Table A.18
0x7402	ATI Target	See Table A.19
0x7403	Fine and Coarse Multipliers	See Table A.20
0x7404	ATI Compensation	See Table A.21
0x7405	Reference Channel Settings 0	See Table A.22
0x7406	Reference Channel Settings 1	See Table A.23
	Channel 5	
0x7500	CRX Select and General Channel Setup	See Table A.17
0x7501	ATI Base and Mode	See Table A.18
0x7502	ATI Target	See Table A.19
0x7503	Fine and Coarse Multipliers	See Table A.20
0x7504	ATI Compensation	See Table A.21

0x7505	Reference Channel Settings 0	See Table A.22
0x7506	Reference Channel Settings 1	See Table A.23
	Channel 6	
0x7600	CRX Select and General Channel Setup	See Table A.17
0x7601	ATI Base and Mode	See Table A.18
0x7602	ATI Target	See Table A.19
0x7603	Fine and Coarse Multipliers	See Table A.20
0x7604	ATI Compensation	See Table A.21
0x7605	Reference Channel Settings 0	See Table A.22
0x7606	Reference Channel Settings 1	See Table A.23
	Channel 7	
0x7700	CRX Select and General Channel Setup	See Table A.17
0x7701	ATI Base and Mode	See Table A.18
0x7702	ATI Target	See Table A.19
0x7703	Fine and Coarse Multipliers	See Table A.20
0x7704	ATI Compensation	See Table A.21
0x7705	Reference Channel Settings 0	See Table A.22
0x7706	Reference Channel Settings 1	See Table A.23
	Hall plate normal	
0x7800	CRX Select and General Channel Setup	See Table A.17
0x7801	ATI Base and Mode	See Table A.18
0x7802	ATI Target	See Table A.19
0x7803	Fine and Coarse Multipliers	See Table A.20
0x7804	ATI Compensation	See Table A.21
0x7805	Reference Channel Settings 0	See Table A.22
0x7806	Reference Channel Settings 1	See Table A.23
	Hall plate inverse	
0x7900	CRX Select and General Channel Setup	See Table A.17
0x7901	ATI Base and Mode	See Table A.18
0x7902	ATI Target	See Table A.19
0x7903	Fine and Coarse Multipliers	See Table A.20
0x7904	ATI Compensation	See Table A.21
0x7905	Reference Channel Settings 0	See Table A.22
0x7906	Reference Channel Settings 1	See Table A.23
Read-Write	**Filter Betas**	
0x7A00	Counts & LTA Filter Beta	See Table A.24
0x7A01	Hall & Fast Filter Beta	See Table A.25
0x7A02	Activated Fast Filter Beta	See Table A.26
Read-Write	**Gesture Settings**	
0x8000	Minimum Gesture Time	See Table A.27
0x8001	Maximum Tap Time	See Table A.28
0x8002	Minimum Hold Time	See Table A.29
0x8003	Tap Delay Time	See Table A.30
0x8004	Tap Gesture Channel Setup	See Table A.31
Read-Write	**Hall Settings**	
0x9000	Bias & Offset Current Settings	See Table A.32
0x9001	Hall Compensation Numerator	See Table A.33
0x9002	Hall Compensation Denominator Low	See Table A.34
0x9003	Hall Compensation Denominator High	See Table A.34
0x9004	Hall Absolute Current Configuration	See Table A.35
Read-Write	**PMU and System Settings**	

0xA0	Control settings	See Table A.36
0xA1	ATI Error Timeout	16-bit value * 0.5 (s)
0xA2	ATI Report Rate	16-bit value (ms)
0xA3	Normal Power Mode Timeout	16-bit value (ms)
0xA4	Normal Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xA5	Low Power Mode Timeout	16-bit value (ms)
0xA6	Low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xA7	Normal Power Update rate in Ultra-low Power Mode	16-bit value (ms)
0xA8	Ultra-low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xA9	ULP Entry Mask	See Table A.37
0xAA	Event Enable	See Table A.38
0xAB	Communication Timeout	See Table A.39
0xAC	General UI Settings 0	See Table A.40
0xAD	General UI Settings 1	See Table A.41
0xAE	Channel Linearisation enable	See Table A.42
0xAF	I^2C Communication	See Table A.43

11 Implementation and Layout

11.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

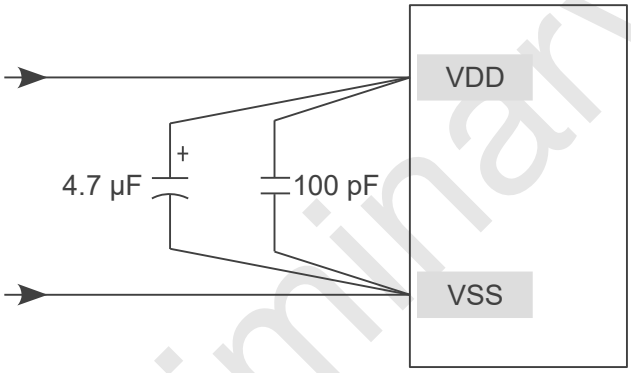


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. The figure below shows an example placement of the VREG capacitors.

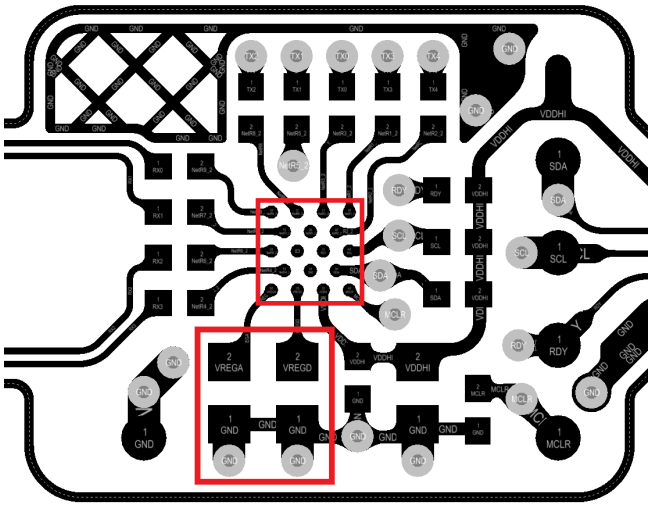


Figure 11.2: VREG Capacitor Placement Close to IC

11.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

11.2 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

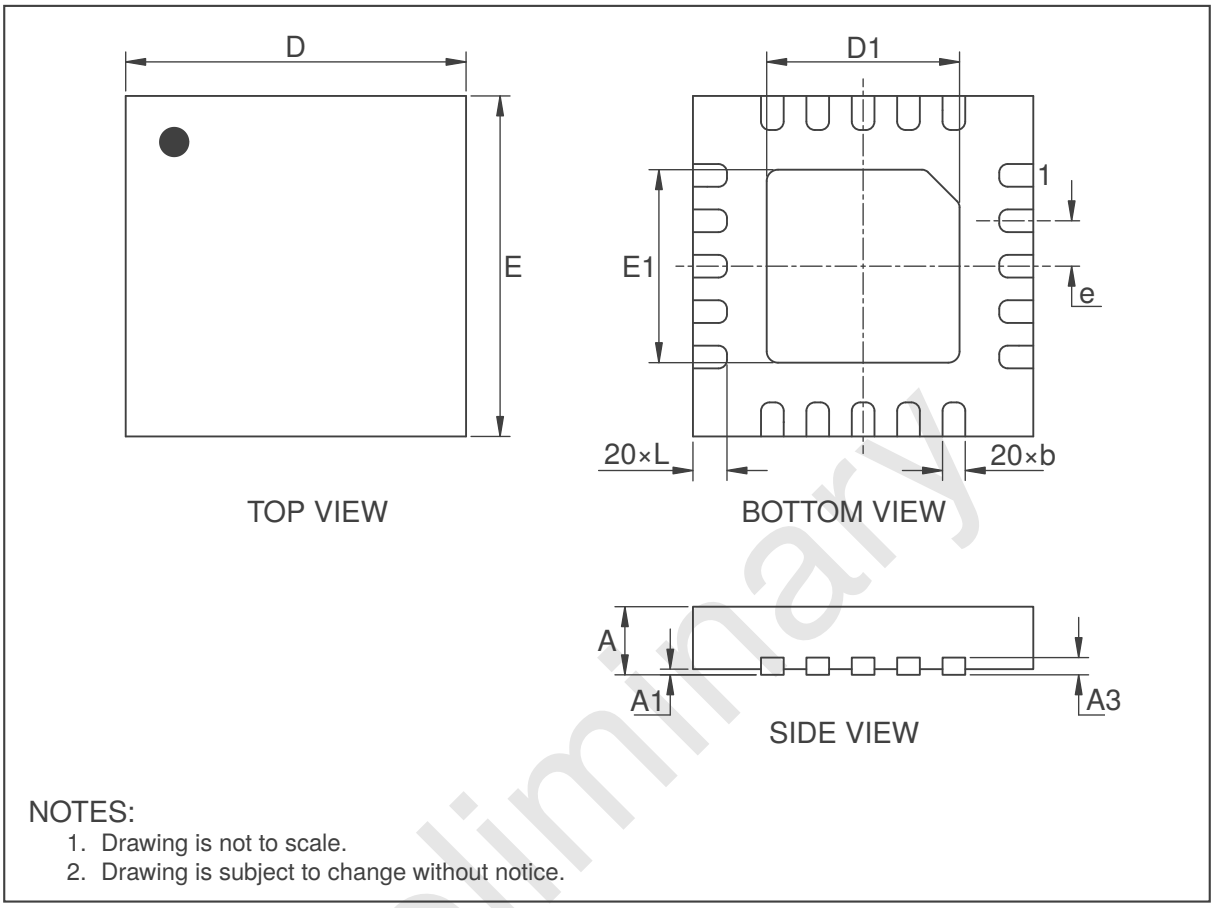
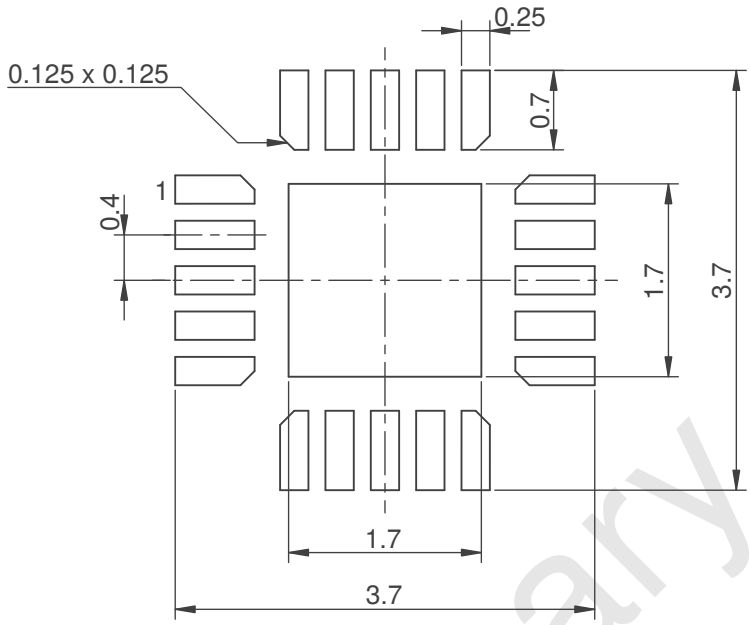


Figure 11.3: QFN (3x3)-20 (QFR) Package Outline Visual Description

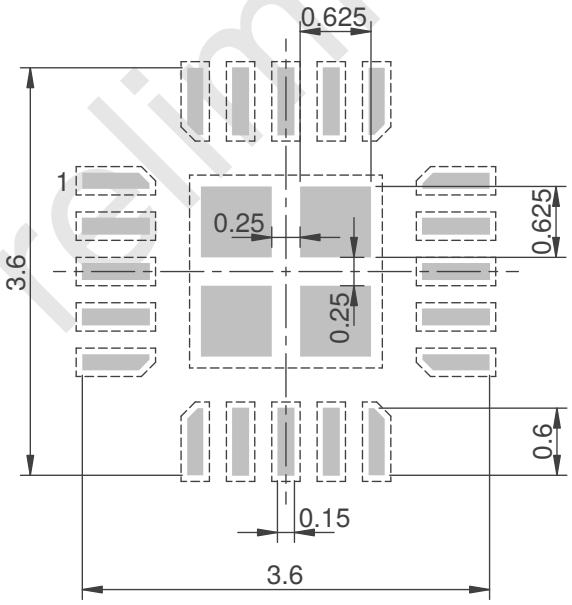
Table 11.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

11.3 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 11.4: QFN (3x3)-20 (QFR) Recommended Footprint

11.4 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

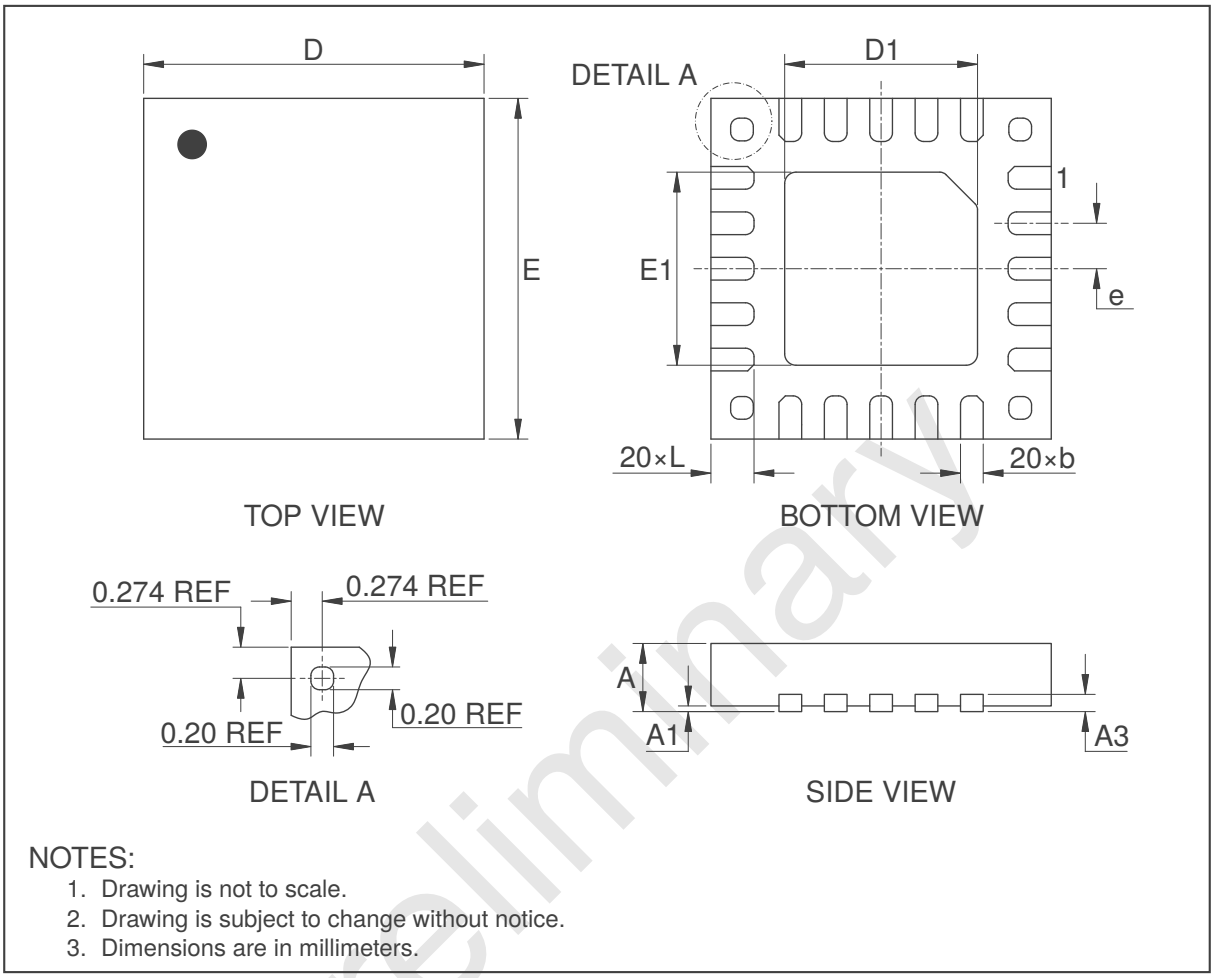
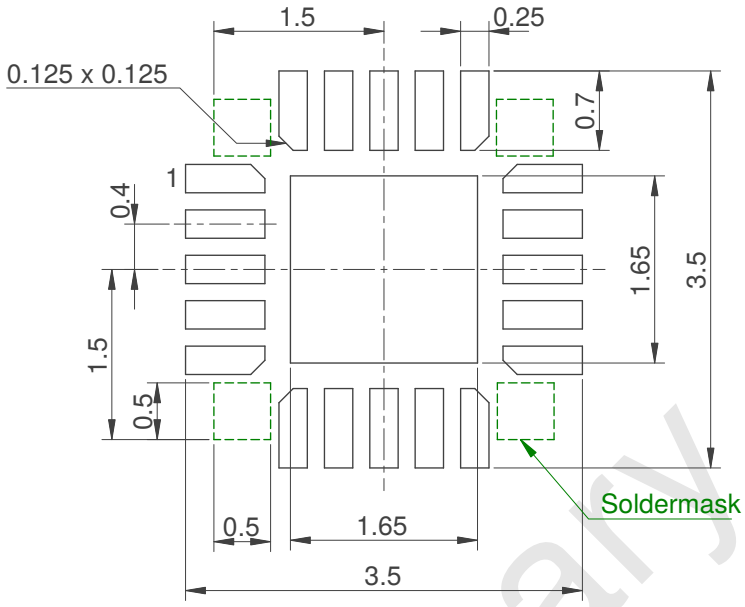


Figure 11.5: QFN (3x3)-20 (QNR) Package Outline Visual Description

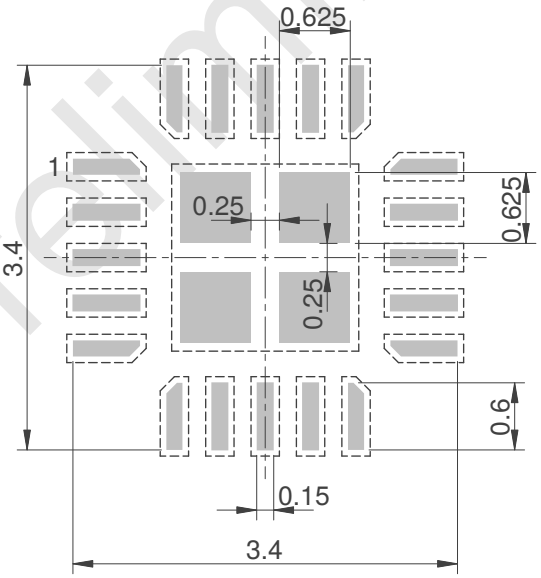
Table 11.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

11.5 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 11.6: QFN (3x3)-20 (QNR) Recommended Footprint

11.6 Package Outline Description – WLCSP18

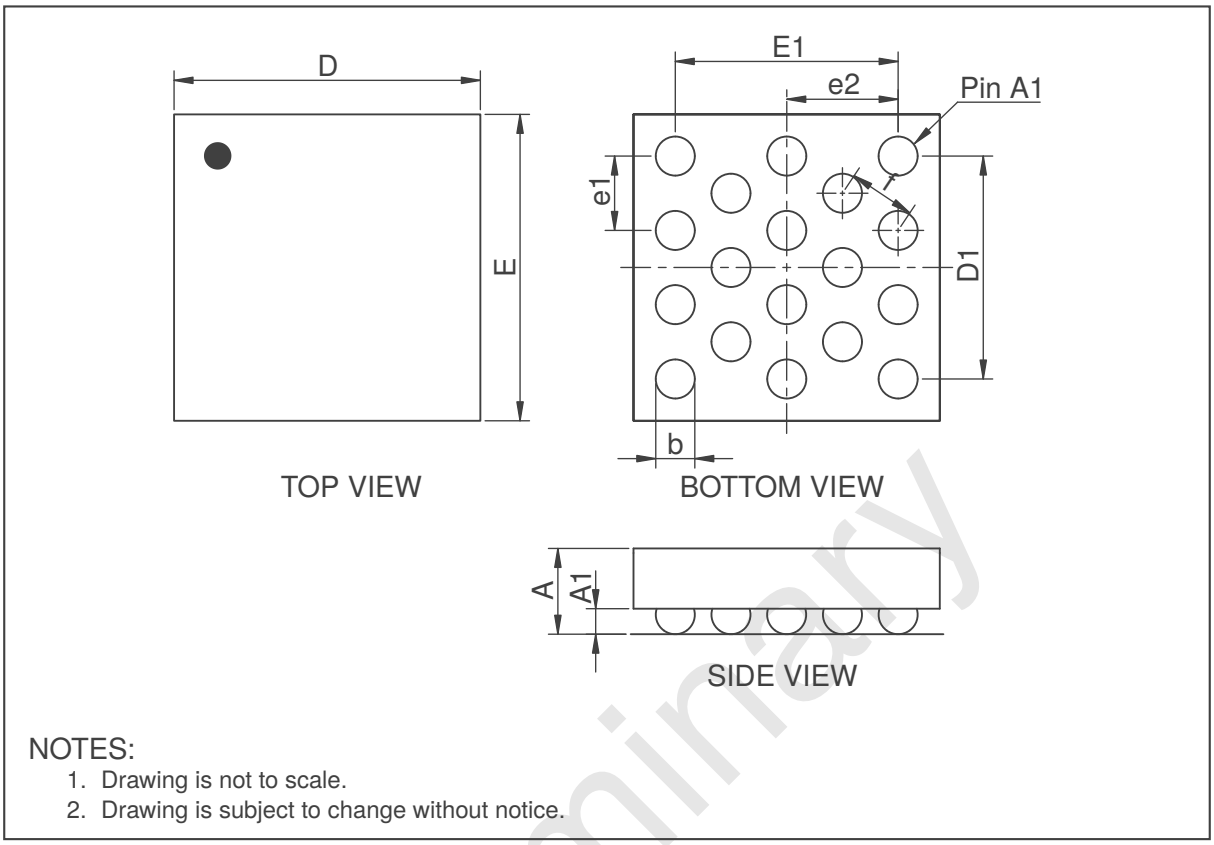
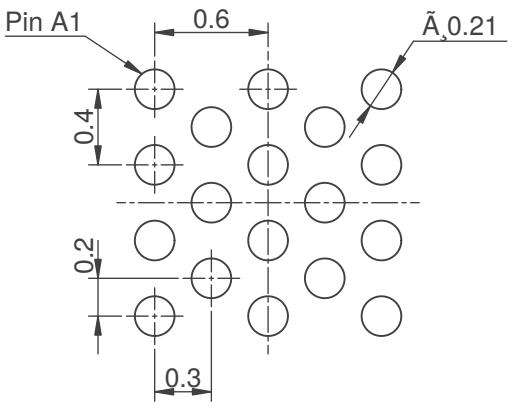


Figure 11.7: WLCSP (1.62x1.62)-18 Package Outline Visual Description

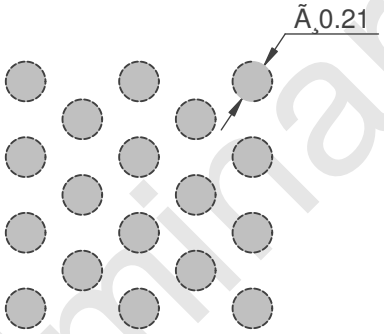
Table 11.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1		1.200 BSC	
E1		1.200 BSC	
e1		0.400 BSC	
e2		0.600 BSC	
f		0.360 REF	

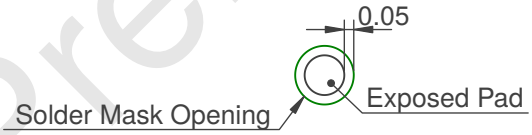
11.7 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



SOLDER MASK BACK-OFF

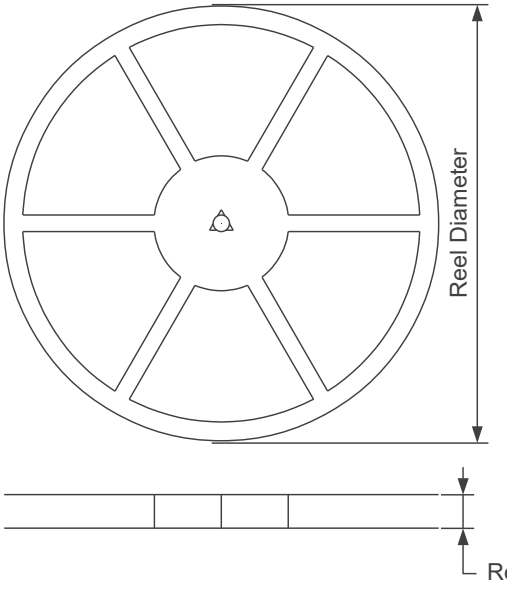
NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

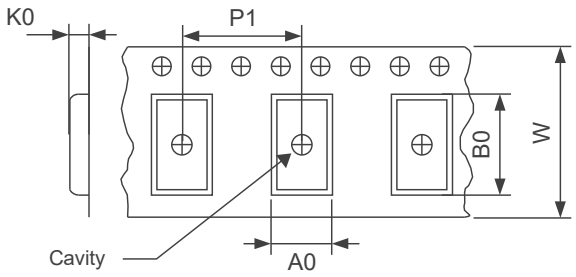
Figure 11.8: WLCSP18 Recommended Footprint

11.8 Tape and Reel Specifications

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

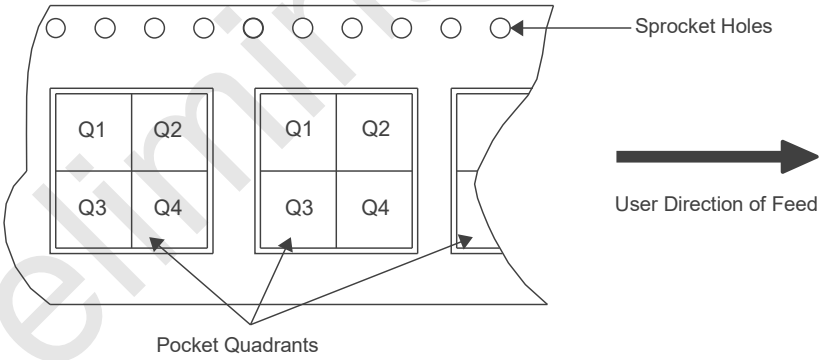


Figure 11.9: Tape and Reel Specification

Table 11.4: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

11.9 Moisture Sensitivity Levels

Table 11.5: Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

11.10 Reflow Specifications

Contact Azoteq

12 Ordering Information

12.1 Ordering Code

IQS7222E zzz ppb

IC NAME	IQS7222E	=	IQS7222E	
			001	Default 0x48 address
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
			QN	QFN-20 package
DEFAULT CONFIGURATION	zzz	=		
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Figure 12.1: Order Code Description

12.2 Top Marking

12.2.1 WLCSP18 Package

Product Name
ppp = product code
xx = batchcode

12.2.2 QFN20 Package Marking Option 1

Product Name
ppp = product code
xx = batchcode

12.2.3 QFN20 Package Marking Option 2

Product Name
ppp = product code
xx = batchcode

13 Package Specification

13.1 Package Outline Description – WLCSP18

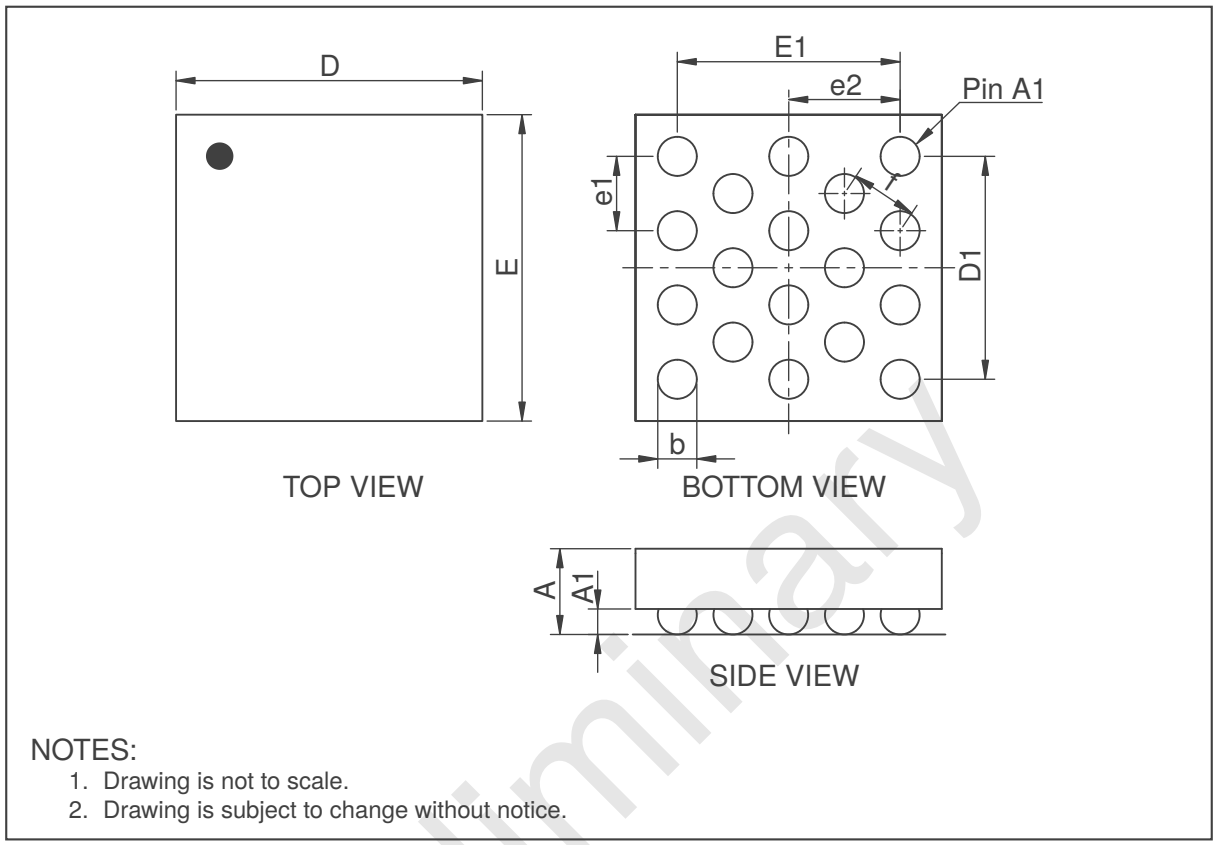
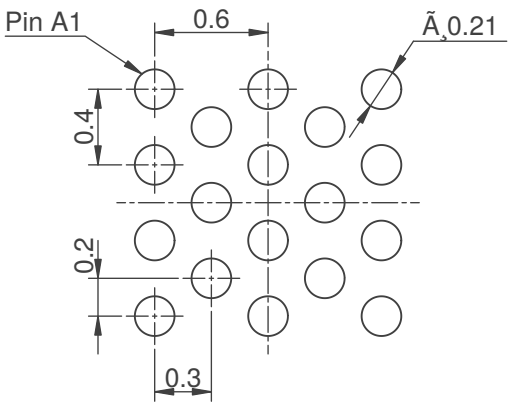


Figure 13.1: WLCSP (1.62x1.62)-18 Package Outline Visual Description

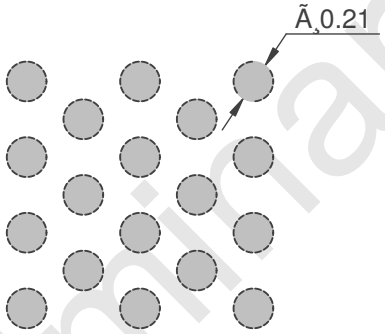
Table 13.1: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1		1.200 BSC	
E1		1.200 BSC	
e1		0.400 BSC	
e2		0.600 BSC	
f		0.360 REF	

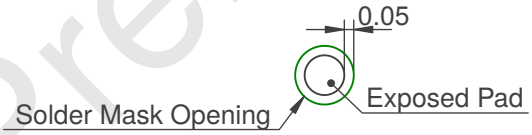
13.2 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.2: WLCSP18 Recommended Footprint

13.3 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

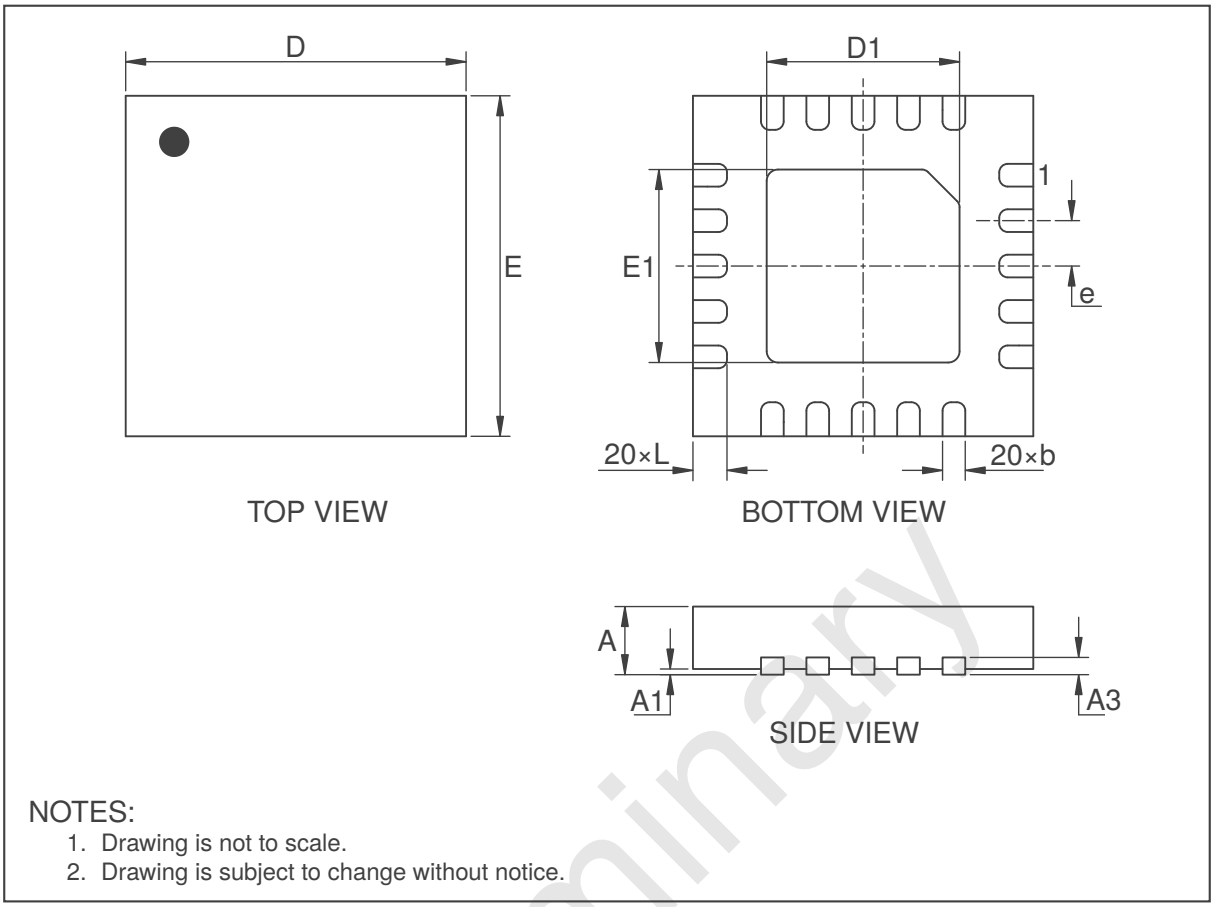
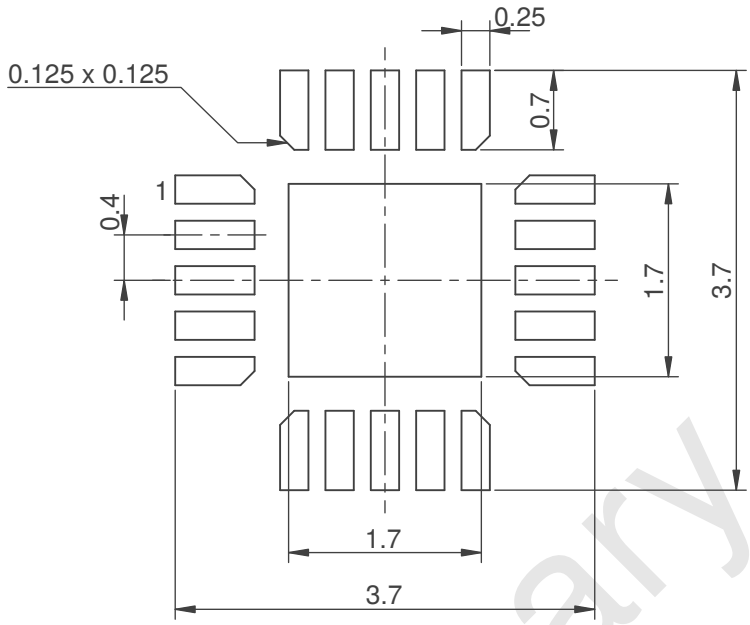


Figure 13.3: QFN (3x3)-20 (QFR) Package Outline Visual Description

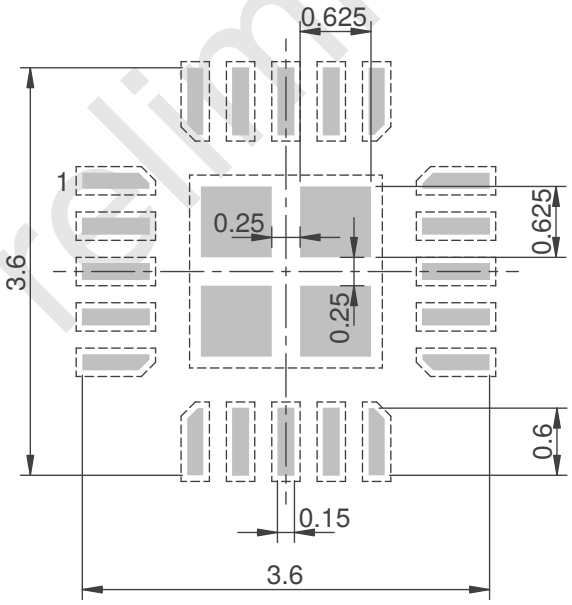
Table 13.2: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

13.4 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.4: QFN (3x3)-20 (QFR) Recommended Footprint

13.5 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

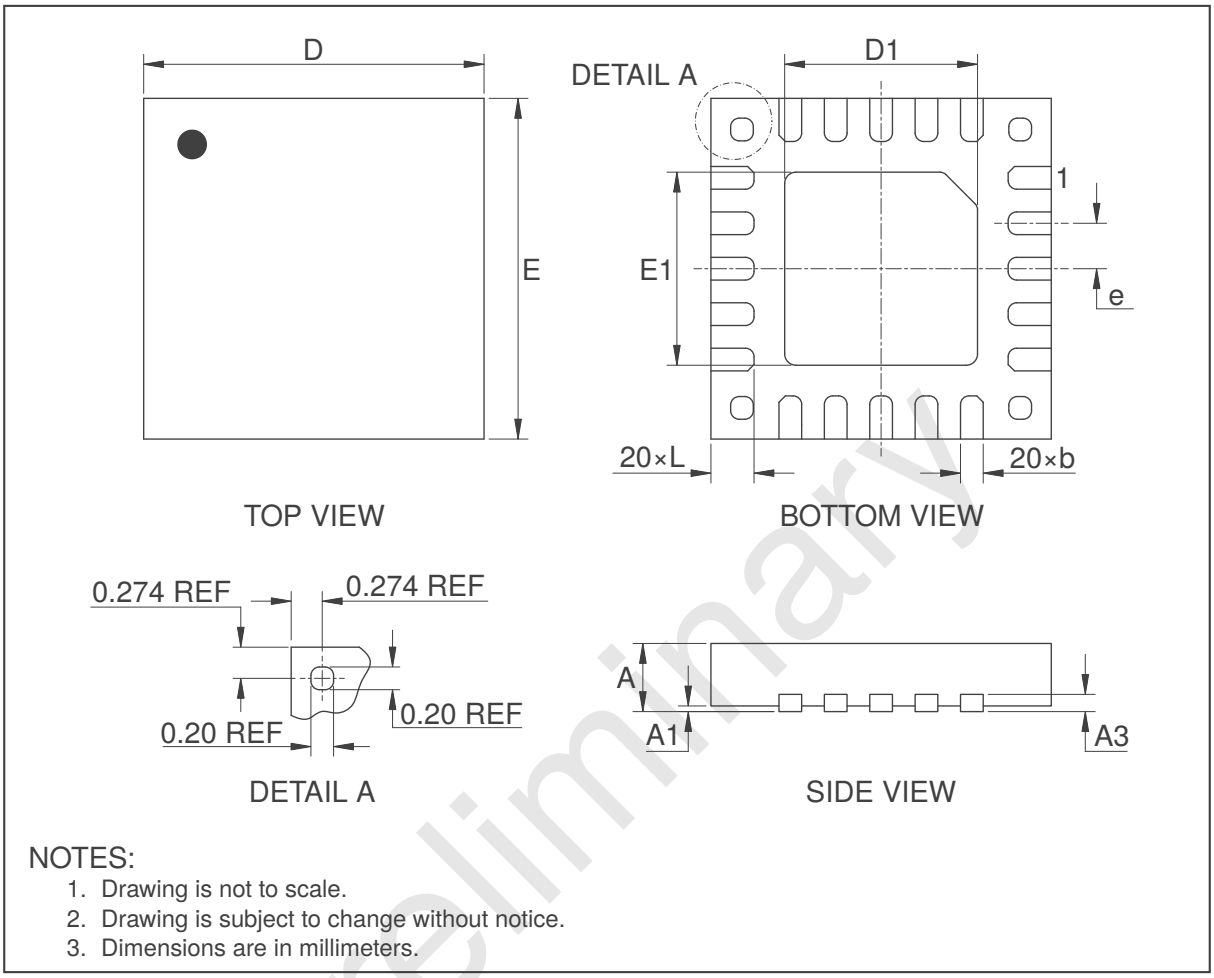
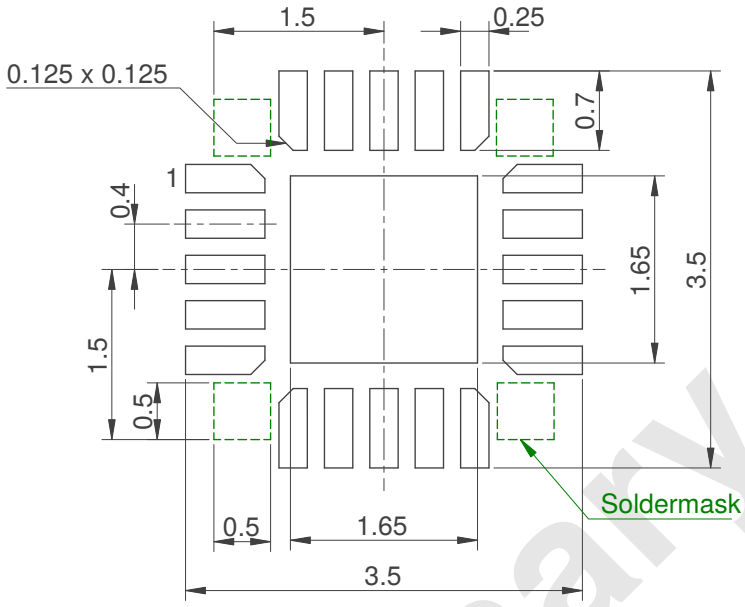


Figure 13.5: QFN (3x3)-20 (QNR) Package Outline Visual Description

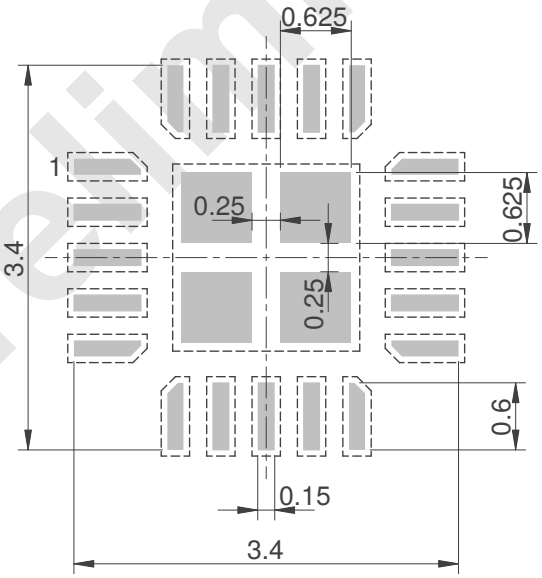
Table 13.3: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

13.6 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



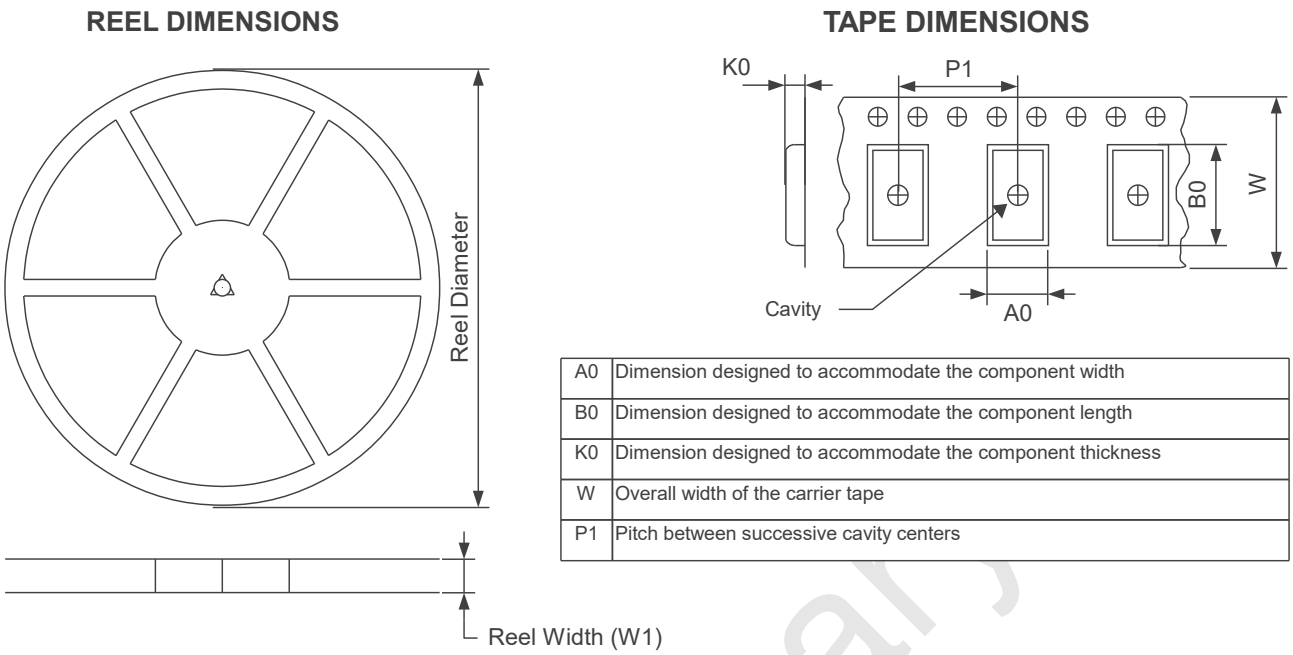
RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 13.6: QFN (3x3)-20 (QNR) Recommended Footprint

13.7 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

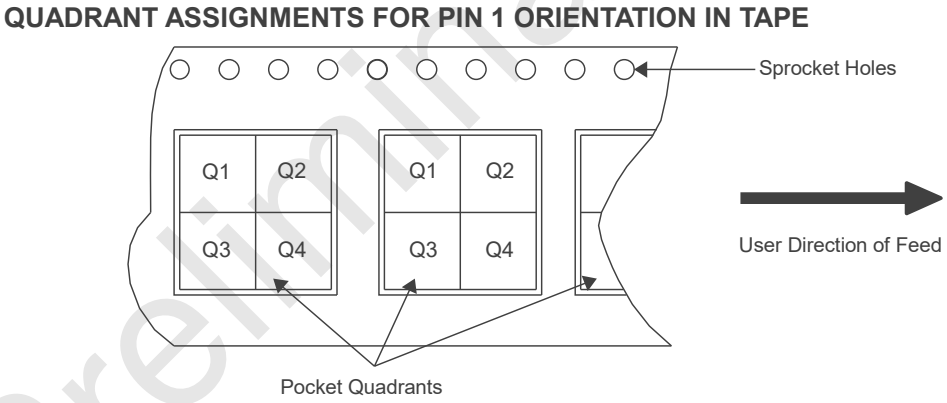


Figure 13.7: Tape and Reel Specification

Table 13.4: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

13.8 Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

13.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Category	Name	Value
0x00	Reserved	Product Number	2383
0x01		Major Version	1
0x02		Minor Version	0
0x03		Reserved	
0x04			
0x05 - 0x09		Reserved	

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved									NP update	Power mode		Reset	Res	ATI Error	ATI Active

- Bit 6: **NP Update**
  - 0: No Normal Power Update occured
  - 1: Normal Power update occured
- Bit 4-5: **Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.3: Events

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Re-served	Gesture Event	Reserved								Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 10: **Gesture Event**
  - 0: No Gesture Event occurred
  - 1: A Gesture Event occurred (either single/double/triple-tap or press-&-hold)
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.4: Proximity Event States

Register: 0x12

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							HALL	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

Table A.5: Touch Event States

Register: 0x13

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
							HALL	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.6: Gesture Event States

Register: 0x40

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
									Event	Temp tap	Busy	Hold	Tap output		

- Bit 6: **Event**
  - 0: No gesture event occurred
  - 1: Gesture event occurred
- Bit 5: **Temp tap**
  - 0: No temporary tap event occurred
  - 1: Temporary tap event occurred
- Bit 4: **Busy**
  - 0: Gesture event detection not busy
  - 1: Gesture event detection busy
- Bit 3: **Hold**
  - 0: No hold event occurred
  - 1: Hold event occurred
- Bit 2-0: **Event**
  - 000: No tap event occurred
  - 001: Single tap event occurred
  - 010: Double tap event occurred
  - 011: Triple tap event occurred

Table A.7: Cycle Setup 0

Register: 0x5000, 0x5100, 0x5200, 0x5300, 0x5400

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 8-15: **Conversion Period**
  - $\frac{128}{FrequencyFraction} - 2$
  - Range: 0 - 127
- Bit 0-7: **Frequency Fraction**
  - $256 * \frac{f_{conv}}{f_{clk}}$
  - Range: 0 - 255
- Note: if Frequency fraction is fixed at 127, the following values of the conversion period will result in the corresponding charge transfer frequencies:
  - 1: 2MHz
  - 5: 1MHz
  - 12: 500kHz
  - 17: 350kHz
  - 26: 250kHz
  - 53: 125kHz

Table A.8: Cycle Setup 1

Register: 0x5001, 0x5101, 0x5201, 0x5301, 0x5401

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	Inactive Rx - GND	Dead time en-abled	FOSC TX Freq	Vbias en-able	PXS Mode		

- Bit 15: **Tx8**
  - 0: Tx8 disabled
  - 1: Tx8 enabled
- Bit 14: **Tx7**
  - 0: Tx7 disabled
  - 1: Tx7 enabled
- Bit 13: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 12: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled
- Bit 11: **Tx4**
  - 0: Tx4 disabled
  - 1: Tx4 enabled
- Bit 10: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 9: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 8: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 7: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled
- Bit 6: **Inactive Rx GND**
  - 0: Inactive Rx floating
  - 1: Inactive Rx Grounded
- Bit 5: **Dead Time Enabled**
  - 0: Deadtime disabled
  - 1: Deadtime enabled
- Bit 4: **TX FOSC Frequency**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Vbias Enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-2: **PXS Mode**
  - 000: None
  - 001: Self-capacitive
  - 010: Mutual capacitance

Table A.9: Cycle Setup 2

Register: 0x5002, 0x5102, 0x5202, 0x5302, 0x5402

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							CTx8-PAT1	CTx7-PAT1	CTx6-PAT1	CTx5-PAT1	CTx4-PAT1	CTx3-PAT1	CTx2-PAT1	CTx1-PAT1	CTx0-PAT1

- Bit 8: **CTx8-PAT1**
  - 0: Tx8 disabled for pattern1
  - 1: Tx8 enabled for pattern1
- Bit 7: **Tx7-PAT1**
  - 0: Tx7 disabled for pattern1

- 1: Tx7 enabled for pattern1

- Bit 6: **Tx6-PAT1**
  - 0: Tx6 disabled for pattern1
  - 1: Tx6 enabled for pattern1
- Bit 5: **Tx5-PAT1**
  - 0: Tx5 disabled for pattern1
  - 1: Tx5 enabled for pattern1
- Bit 4: **Tx4-PAT1**
  - 0: Tx4 disabled for pattern1
  - 1: Tx4 enabled for pattern1
- Bit 3: **Tx3-PAT1**
  - 0: Tx3 disabled for pattern1
  - 1: Tx3 enabled for pattern1
- Bit 2: **Tx2-PAT1**
  - 0: Tx2 disabled for pattern1
  - 1: Tx2 enabled for pattern1
- Bit 1: **Tx1-PAT1**
  - 0: Tx1 disabled for pattern1
  - 1: Tx1 enabled for pattern1
- Bit 0: **Tx0-PAT1**
  - 0: Tx0 disabled for pattern1
  - 1: Tx0 enabled for pattern1

Table A.10: Global Cycle Setup

Register: 0x5500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	RF Filter EN	Maximum counts		1	0	0	0	Auto Mode		Reserved	

- Bit 10: **RF Filter Enable**
  - 0: RF Filter disabled
  - 1: RF Filter enabled
- Bit 8-9: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 2-3: **Auto Mode**
  - Number of conversions created before each interrupt is generated
  - 00: 4
  - 01: 8
  - 10: 16
  - 11: 32

Table A.11: Coarse and Fine Multipliers Preload

Register: 0x5501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Multiplier Preload					Reserved				Coarse Multiplier Preload				

- Bit 0-4: **Coarse Multiplier Preload**
  - 5-bit coarse multiplier preload value
- Bit 9-13: **Fine Multiplier Preload**
  - 5-bit fine multiplier preload value

Table A.12: ATI Compensation Preload

Register: 0x5502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ATI Compensation Preload									

- Bit 0-9: **ATI Compensation Preload**
  - 10-bit preload value

Table A.13: Button Setup 0

Register: 0x6000, 0x6100, 0x6200, 0x6300, 0x6400, 0x6500, 0x6600, 0x6700, 0x6800

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 8-11: **Enter Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 0-7: **Proximity Threshold**
  - 8-bit value

Table A.14: Button Setup 1

Register: 0x6001, 0x6101, 0x6201, 0x6301, 0x6401, 0x6501, 0x6601, 0x6701, 0x6801, 0x6901

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{LTA}{256}$*Threshold bit value - $\frac{LTA}{2^{16}}$*Hysteresis bit value
- Bit 0-7: **Touch Threshold**
  - $\frac{LTA}{256} * 8\text{bit value}$

Table A.15: Button Setup 2

Register: 0x6002, 0x6101, 0x6202, 0x6302, 0x6402, 0x6502, 0x6602, 0x6702, 0x6802, 0x6902

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Event Timeout								Prox Event Timeout							

- Bit 8-15: **Touch Event Timeout**
  - 8-bit value * 500ms
  - 0: Never timeout (recommended for use with follower and reference channels)
- Bit 0-7: **Prox Event Timeout**
  - 8-bit value * 500ms
  - 0: Never timeout (recommended for use with follower and reference channels)

Table A.16: CRX Select and General Channel Setup(CH0-CH4)

Register: 0x7000, 0x7100, 0x7200, 0x7300, 0x7400

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode		ATI Band		Sensor type	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs 80pF	0v5 Rev	Proj Bias Select	

- Bit 14-15: **Mode**
  - 00: Independent
  - 01: Reference
  - 10: Follower
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Sensor type**
  - 0: Capacitive
  - 1: Hall
- Bit 10: **Invert Direction**
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional**
  - 0: Bi-directional sensing disabled

- 1: Bi-directional sensing enabled

- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled
- Bit 6: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled
- Bit 5: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled
- Bit 4: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled
- Bit 3: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vbias enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-1: **Mutual Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.17: CRX Select and General Channel Setup(CH5-CH7)

Register: 0x7500, 0x7600, 0x7700, 0x7800, 0x7900

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode		ATI Band		Sensor type	Invert	Dual	Enabled	CRX7	CRX6	CRX5	CRX4	Cs 80pF	0v5 Rev	Proj Bias Select	

- Bit 14-15: **Mode**
  - 00: Independent
  - 01: Reference
  - 10: Follower
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Sensor type**
  - 0: Capacitive
  - 1: Hall
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled
- Bit 6: **CRx6**
  - 0: CRx6 disabled
  - 1: CRx6 enabled

- Bit 5: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled
- Bit 4: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled
- Bit 3: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vbias enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-1: **Mutual Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.18: ATI Base and Mode

Register:	0x7001, 0x7101, 0x7201, 0x7301, 0x7401, 0x7501, 0x7601, 0x7701, 0x7801, 0x7901															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Coarse offset slect				Fine offset select				ATI Base					ATI Mode		

- Bit 12-15: **Coarse offset select**
  - Coarse offset current in 3 µA steps.
  - Range: −21 µA to 21 µA (MSB bit15 is sign bit).
- Bit 8-12: **Fine offset select**
  - Fine offset current in 200 nA steps.
  - 4-bit value * 200 nA.
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

Table A.19: ATI Target

Register:	0x7002, 0x7102, 0x7202, 0x7302, 0x7402, 0x7502, 0x7602, 0x7702, 0x7802, 0x7902															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target															

- Bit 0-15: **ATI Target**
  - 16-bit value

Table A.20: Fine and Coarse Multipliers

Register:	0x7003, 0x7103, 0x7203, 0x7303, 0x7403, 0x7503, 0x7603, 0x7703, 0x7803, 0x7903															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.21: ATI Compensation

Register:	0x7004, 0x7104, 0x7204, 0x7304, 0x7404, 0x7504, 0x7604, 0x7704, 0x7804, 0x7904														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.22: Reference Channel Settings 0

Register:	0x7005, 0x7105, 0x7205, 0x7305, 0x7405, 0x7505, 0x7605, 0x7705, 0x7805, 0x7905														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Follower Mask Link Ptr/ Reference Sensor Ptr															

- Please note that the register value is used for either Follower Mask Link Ptr or Reference Sensor Ptr based on the mode selected in table A.16 / A.17, bit 14-15
- **Follower Mask Link Pointer** - Mode = Reference
  - Do not care (not used): Prox (always)
- **Reference Sensor Pointer** - Mode = Follower
  - 0x000 (decimal = 0): None
  - 0x418 (decimal = 1048): Channel 0
  - 0x44A (decimal = 1098): Channel 1
  - 0x47C (decimal = 1148): Channel 2
  - 0x4AE (decimal = 1198): Channel 3
  - 0x4E0 (decimal = 1248): Channel 4
  - 0x512 (decimal = 1298): Channel 5
  - 0x544 (decimal = 1348): Channel 6
  - 0x576 (decimal = 1370): Channel 7
  - 0x5A8 (decimal = 1448): Hall

Table A.23: Reference Channel Settings 1

Register:	0x7005, 0x7105, 0x7205, 0x7305, 0x7405, 0x7505, 0x7605, 0x7705, 0x7805, 0x7905														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Follower Mask/ Reference Sensor Weight															

- Please note that the register value is used for either Follower Mask or Reference Weight based on the mode selected in table A.16 / A.17, bit 14-15
- **Follower Mask** (used to enable current sensor as a reference channel for the selected channel) - Mode = Reference
  - 0: Disabled
  - 1: Channel enabled as reference for Channel 0
  - 2: Channel enabled as reference for Channel 1
  - 4: Channel enabled as reference for Channel 2
  - 8: Channel enabled as reference for Channel 3
  - 16: Channel enabled as reference for Channel 4
  - 32: Channel enabled as reference for Channel 5
  - 64: Channel enabled as reference for Channel 6
  - 128: Channel enabled as reference for Channel 7
  - 256: Channel enabled as reference for Hall
- **Reference Weight** - Mode = Follower
  - 16-bit decimal value/256

Table A.24: Filter Betas

Register:	0x7A00														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Low Power Beta				LTA Normal Power Beta				Counts Low Power Beta				Counts Normal Power Beta			

- Bit 12-15: **LTA Low Power Beta Filter Value**

- 4-bit value

- Bit 8-11: **LTA Normal Power Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Counts Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Counts Normal Power Beta Filter Value**
  - 4-bit value

Table A.25: Fast Filter Betas

Register: 0x7A01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hall Reference Beta				Hall Delta Beta				LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- Bit 12-15: **Hall Reference Beta Filter Value**
  - 4-bit value
- Bit 8-11: **Hall Delta Beta Filter Value**
  - 4-bit value
- Bit 4-7: **LTA Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
  - 4-bit value

Table A.26: Activated Filter Betas

Register: 0x7A02

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Acitvated Low Power Beta				Activated Normal Power Beta			

- Bit 4-7: **Activated Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Activated Normal Power Beta Filter Value**
  - 4-bit value

Table A.27: Minimum Gesture Time

Register: 0x8000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Minimum Gesture Time [ms]															

- Bit 0-15: **Minimum Gesture Time**
  - 16-bit value [ms]

Table A.28: Maximum Tap Time

Register: 0x8001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Maximum Tap Time [ms]															

- Bit 0-15: **Maximum Tap Time**
  - 16-bit value [ms]

Table A.29: Minimum Hold Time

Register: 0x8002

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Minimum Hold Time [ms]															

- Bit 0-15: **Minimum Hold Time**
  - 16-bit value [ms]

Table A.30: Tap Delay Time

Register: 0x8003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tap Delay Time [ms]															

- Bit 0-15: **Tap Delay Time**
  - 16-bit value [ms]

Table A.31: Tap Gesture Channel Setup

Register: 0x8004

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												Boolean OR	Boolean AND	CH1	CH0

- Bit 3: **Boolean OR**
  - 0: No use
  - 1: Either CH1 OR CH0 delta can satisfy gesture
- Bit 2: **Boolean AND**
  - 0: No use
  - 1: Both CH1 AND CH0 delta should satisfy gesture requirements
- Bit 1: **CH1**
  - 0: CH1 disabled for gestures
  - 1: CH1 enabled for gestures
- Bit 0: **CH0**
  - 0: CH0 disabled for gestures
  - 1: CH0 enabled for gestures

Table A.32: Hall Current Settings

Register: 0x9000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hall Bias Current								Hall Offset Current							
Boost Gain	Bias level			Bias trim				Offset sign	Offset level			Offset trim			

- Bit 15: **Boost Gain**
  - 0: Disable boost gain ($15.7\,\frac{nA}{mT}$)
  - 1: Enable boost gain ($62\,\frac{nA}{mT}$)
- Bit 12-14: **Hall bias current level**
  - 3-bit value: 8 levels between 550 µA - 1.2 mA
- Bit 8-11: **Hall bias current trim**
  - 4-bit value: 16 levels (±3% per step)
- Bit 7: **Offset sign**
  - 0: Negative offset current
  - 1: Positive offset current
- Bit 4-6: **Hall bias current level**
  - 3-bit value: 8 levels between 0 µA - 21 µA
- Bit 0-3: **Hall bias current trim**
  - 4-bit value: 16 levels (200 nA per step)

Table A.33: Hall Compensation numerator

Register: 0x9001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hall Compensation Numerator															

- Bit 0-15: **Hall Compensation Numerator**
  - 16-bit value: Hall Compensation Numerator

Table A.34: Hall Compensation Denominator

Register: 0x9002, 0x9003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hall Compensation Denominator Low															
Hall Compensation Denominator High															

- Bit 0-31: **Hall Compensation Denominator** (High [0x9003 « 16] | Low [0x9002]])
  - 32-bit value: Hall Compensation Denominator

Table A.35: Absolute Current Configuration

Register: 0x9004

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Absolute Current Configuration															

- Bit 0-15: **Absolute Current Configuration**
  - Reserved maintain the default setup value

Table A.36: Control Settings

Register: 0xA0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Setup com-plete	Interface type	Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 7: **Setup complete**
  - 0: Setup can/should be configured before setting this bit. SETUP output will be HIGH.
  - 1: Set to acknowledge that the device setup is completed. SETUP output will be set LOW. Conversions active.
- Bit 6: **Interface Selection**
  - 0: I^2C streaming
  - 1: I^2C event mode
- Bit 4-5: **Power Mode Selection**
  - 00: Normal Power
  - 01: Low Power
  - 10: Ultra-low Power
  - 11: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
- Bit 1: **Soft Reset**
  - 0: Do not reset device
  - 1: Reset device after communication window terminates
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.37: Channel ULP entry mask

Register: 0xA9

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							HALL	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Please note that all channels required to enter ULP with an active prox/touch state, must be unmasked/cleared in this register.
- Bit 9-15: **Reserved**
  - Reserved
- Bit 0-8: **Channel ULP entry mask**
  - 0: Unmasked, ULP can be entered if channel(s) has active prox/touch state.
  - 1: Channel prox/touch activation will prevent ULP entry.
  - bit8 = 0: Hall activation is required to enter ULP mode (ULP cycle conversion in selected plate direction).

Table A.38: Event Enable

Register: 0xAA

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power event	ATI event	Re-served	Gesture event	Reserved								Touch event	Prox event

- Bit 13: **Power Event**
  - 0: Power event masked

- 1: Power event enabled

- Bit 12: **ATI Event**
  - 0: ATI event masked
  - 1: ATI event enabled
- Bit 10: **Gesture Event**
  - 0: Geture event masked
  - 1: Gesture event enabled
- Bit 1: **Touch Event**
  - 0: Touch event masked
  - 1: Touch event enabled
- Bit 0: **Prox Event**
  - 0: Prox event masked
  - 1: Prox event enabled

Table A.39: I²C Communication Timeout

Register:	0xAB														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I²C Communication Timeout															

- Bit 0-15: **I²C Communication Timeout**
  - 16-bit value [ms]
  - Default = 500ms

Table A.40: General UI Settings 0

Register:	0xAC														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Release Delta Percentage								Activation settling threshold							

- Bit 8-15: **Release Delta Percentage**
  - 8-bit value
  - Release Delta Percentile $= \frac{ReleaseDeltaPercentage}{127} * 100[\%]$
  - Default = $10'd/127 * 100\% = 8\%$
- Bit 0-7: **Activation settling threshold**
  - 8-bit value
  - Activation settling threshold [counts]
  - Default = 20 counts

Table A.41: General UI Settings 1

Register:	0xAD														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Delta Snap-shot Sample Delay							

- Bit 8-15: **Reserved**
  - Reserved
- Bit 0-7: **Delta Snap-shot Sample Delay**
  - 8-bit value [samples in current power mode]
  - Default = 20 samples

Table A.42: Channel Linearisation Enable

Register:	0xAE														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Please note that all channels required to be linearised, must be enabled by setting the corresponding channel's linearisation enable bit in this register.
- Bit 8-15: **Reserved**
  - Reserved
- Bit 0-7: **Channel Linearisation Enable**
  - 0: Disabled, channel counts not linearised.
  - 1: Enabled, channel counts are linearised by taking $\frac{1}{Raw_{counts}} * (ATI_{target})$.

Table A.43: I²C Communication

Register:		0xAF													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												Stop received	Start received	RW check disabled	Stop bit disabled

- Bit 4-15: **Reserved**
  - Reserved
- Bit 3: **Stop Received Flag**
  - 0: No I²C stop received
  - 1: I²C stop received
- Bit 2: **Start Received Flag**
  - 0: No I²C start received
  - 1: I²C start received
- Bit 1: **RW Check Disabled**
  - 0: Write not allowed to read only registers
  - 1: Read and write allowed to read only registers
- Bit 0: **Stop Bit Disabled**
  - 0: I²C communication window terminated by stop bit.
  - 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window

B Revision History

Release	Date	Changes
v1.0	29 July 2024	Official release

Contact Information

	USA	Asia	South Africa
Physical Address	11940 Jollyville Suite 120-S Austin TX 78759 USA	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC	1 Bergsig Avenue Paarl 7646 South Africa
Postal Address	11940 Jollyville Suite 120-S Austin TX 78759 USA	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC	PO Box 3534 Paarl 7620 South Africa
Tel	+1 512 538 1995	+86 755 8303 5294 ext 808	+27 21 863 0033
Email	info@azoteq.com	info@azoteq.com	info@azoteq.com

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